GOWIN
PROGRAMMING FOR FUTURE

GW1N series FPGA Products

Data Sheet

DS100-1.08E,2016-07-22

Notice of Disclaimer

Revision History

Data	Version	Desription
2016/06/27	1.07E	Initial version.
2016/7/22	1.08E	Update the graphics.

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1 About This Guide

1.1 Purpose

This data sheet mainly describes the features, product resources and structure, AC/DC characteristic, timing specification of configuration interface, and the ordering information of GW1N series FPGA product, which helps you to understand the GW1N series FPGA products quickly and helps you with the device selection and usage.

1.2 Supported Products

The information in this guide applies to the following products:

GW1N series FPGA products: GW1N-1, GW1N-2, GW1N-4, GW1N-6, and GW1N-9.

1.3 Related Documents

The latest user guides are available on our Website. Refer to the related documents via http://www.gowinsemi.com.cn:

1. GW1N series FPGA Products Data Sheet (DS100-1.10)
2. GW1N series FPGA Products Programming and Configureation User Guide (UG100-1.07)
3. GW1N series FPGA Products Package and Pinout (UG103-1.10);
4. GW1N-1 Pinout (UG101-1.07)
5. GW1N-2&4 Pinout (UG105-1.10)

1.4 Abbreviations and Terminology

Table 1-1 lists the abbreviations and terminologies used in this manual.

Table 1-1 Abbreviations and Terminologies

Abbreviation/ Terminology	Full Name	Meaning
FPGA	Field Programmable Gate Array	-
CFU	Configurable Function Unit	-
CLS	Configurable Logic Slice	-
CRU	Configurable Routing Unit	-
LUT4	4-input Look-up Tables	-
LUT5	5-input Look-up Tables	-
LUT6	6-input Look-up Tables	-
LUT7	7-input Look-up Tables	-
LUT8	8-input Look-up Tables	-
REG	Register	-
ALU	Arithmetic Logic Unit	-
IOB	Input/Output Block	-
S-SRAM	Shadow SRAM	-
B-SRAM	Block SRAM	-
SP	Single Port	-
SDP	Semi Dual Port	-
DP	Dual Port	-
DSP	Digital Signal Processing	-
DQCE	Dynamic Quadrant Clock Enable	-
DCS	Dynamic Clock Selector	-
PLL	Phase-locked Loop	-
DLL	Delay-locked Loop	
CS30	WLCSP30	WLCSP30 package
CS72	WLCSP72	WLCSP72 package
QN32	QFN32	QFN32 package
LQ100	LQFP100	LQFP100 package
LQ144	LQFP144	LQFP144 package
MG160	MBGA160	MBGA160 package
PG204	PBGA204	PBGA204 package
PG256	PBGA256	PBGA256 package
UG332	UBGA332	UBGA332 package
TDM	Time Division Multiplexing	-

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If any questions, comments, or suggestions, please feel free to contact us directly.

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2General Description

GW1N series FPGA products is the first generation products of LittleBee® family, which contains the features of low power consumption, instant on, low cost, non-volatile, high security, various packages, and flexible usage.

Gowin Semiductor provides a tool FPGA designer. This supports GW1N series FPGA products and can be used for FPGA synthesizing, layout, place and routing, data bitstream generation and download, etc.

2.1 Features

- User Flash
  - Up to 1,792Kbits
  - 10,000 write cycles
- Lower Power Consumption
  - 55nm embedded flash technology
  - LV: supports 1.2V core voltage
  - UV: built-in linear regulator, supports1.8V, 2.5V, and 3.3V core voltage input
  - Clock dynamically turning on/ turning off
- Mutiple I/O Standards

  LVCMOS33/25/18/15/12; LVTTL33, SSTL33/25/18 I, SSTL33/25/18 II, SSTL15; HSTL18 I, HSTL18 II, HSTL15 I; PCI, LVDS25, RSDS, LVDS25E, BLVDSE

  MLVDSE, LVPECLE, RSDSE
  - Input hysteresis option
  - Supports 4mA,8mA,16mA,24mA,etc. drive options
  - Output Slew Rate options
  - Output drive strength option
  - Individual Bus Keeper, Weak Pull-up, Weak Pull-down, and Open Drain option
  - Hot Socket

- High Performance DSP
  - High performance digital signal processing ability
  - Supports 9 x 9,18 x 18,36 x 36bit multiplier and 54bit accumulator;
  - Multipliers cascading
  - Registers pipeline and bypass
  - Adaptive filtering through signal feedback
  - Supports barrel shifter
- Abundant Slices
  - 4 input LUT (LUT4)
  - Double-edge flip-flops
  - Supports shift register and distributed register
- Block SRAM with Multiple Modes
  - Supports Dual Port, Single Port, and Semi Dual Port
  - Supports bytes write enable
- Flexible PLLs+DLLs
  - Frequency adjustment (multiply and division) and phase adjustment
  - Supports global clock
- Built-in Flash Programming
  - Instant-on
  - Supports security bit operation
  - Supports AUTO BOOT and DUAL BOOT
- Configuration
  - JTAG configuration
  - Up to 6 GowinCONFIG configuration modes: AUTOBOOT, SSPI, MSPI, CPU, SERIAL, DUAL BOOT

2.2 Product Resources

Table 2-1 Product Resources

Device	GW1N-1	GW1N-2	GW1N-4	GW1N-6	GW1N-9
LUT4	1,152	2,304	4,608	6,912	8,640
Flip-Flop (FF)	864	1,728	3,456	5,184	6,480
S-SRAM (bits)	0	0	0	13,824	17,280
B-SRAM (bits)	72K	180K	180K	468K	468K
B-SRAM Number	4	10	10	26	26
User Flash (bits)	96K	220K	220K	1,792K	1,792K
18 x 18 Multiplier	0	16	16	20	20
PLLs+DLLs	0	2+2	2+2	2+3	2+3
I/O Bank Number	4	4	4	4	4
Max. User I/O	121	204	204	272	272
Core Voltage (LV)	1.2V	1.2V	1.2V	1.2V	1.2V
Core Voltage (UV)	1.8/2.5/ 3.3V	1.8/2.5/ 3.3V	1.8/2.5/ 3.3V	1.8/2.5/ 3.3V	1.8/2.5/ 3.3V

2.3 Package Information

Table 2-2 Package Information and Max. I/O

Package[1]	Pitch (mm)	Size (mm^2)	GW1N-1	GW1N-2[3]	GW1N-4[3]	GW1N-6[3]	GW1N-9[3]
CS30	0.4	2.4 x 2.3	23	-	-	-	-
CS72	0.4	3.6 x 3.3	-	57[2]	57[2]	-	-
QN32	0.5	5 x 5	23	23	23	-	-
LQ100	0.5	14 x 14	79[2]	79[2]	79[2]	-	-
LQ144	0.5	20 x 20	118[2]	118[2]	118[2]	118[2]	118[2]
MG160	0.5	8 x 8	121[4]	129[4]	129[4]	129[4]	129[4]
PG204	1.0	17 x 17	121	-	-	-	-
PG256	1.0	17 x 17	-	205[2]	205[2]	205[2]	205[2]
UG332	0.8	17 x 17	-	-	-	272[3]	272[3]

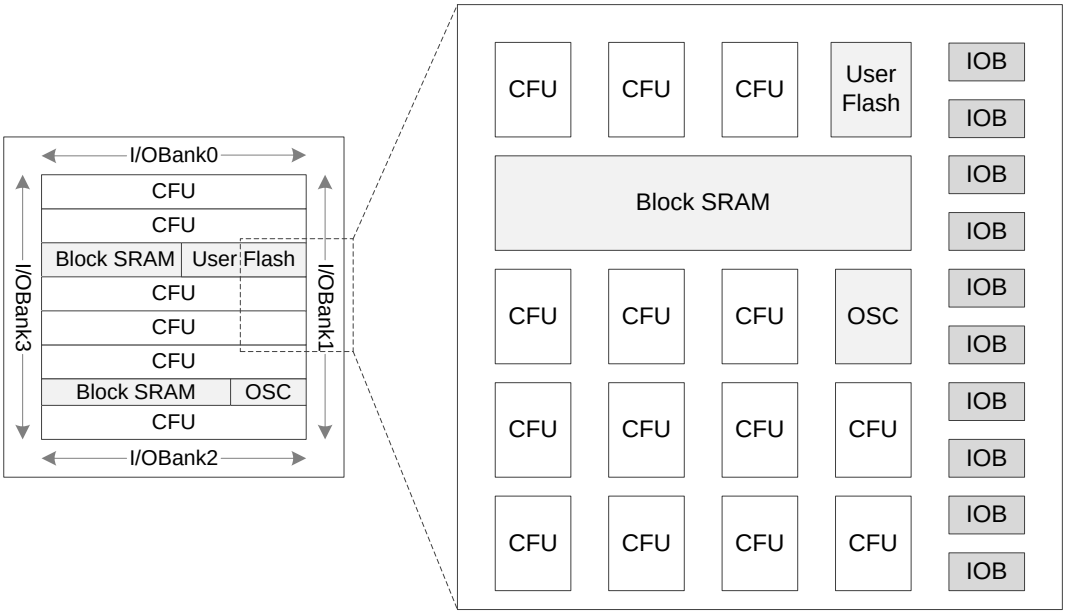
Note!

- [1] The package types in this data sheet are written with abbreviations. See *5.1 Part Name*.
- [2] ⟷ means the various devices pins are compatible when the package types are same.
- [3]GW1N-2 pins and GW1N-4 pins are entirely compatible; GW1N-6 pins and GW1N-9 pins are entirely compatible.
- [4]For the package type MG160, GW1N-1 pins, GW1N-2 pins, and GW1N-4 pins are compatible, but GW1N-1 I/O pins are fewer releatively. Please refer to *GW1N series FPGA products Pinout* for the detailed information.

3 Architecture

3.1 Architecture Overview

Figure 3-1 GW1N-1 Architecture Overview



As shown above, the core of GW1N-1 is CFU. GW1N-1 also prvides 4 B-SRAM, 96Kbits user Flash, and on chip oscillator, and supports Instant-on. See Table 2-1for the detailed information.

Figure 3-2 GW1N-4 Architecture Overview

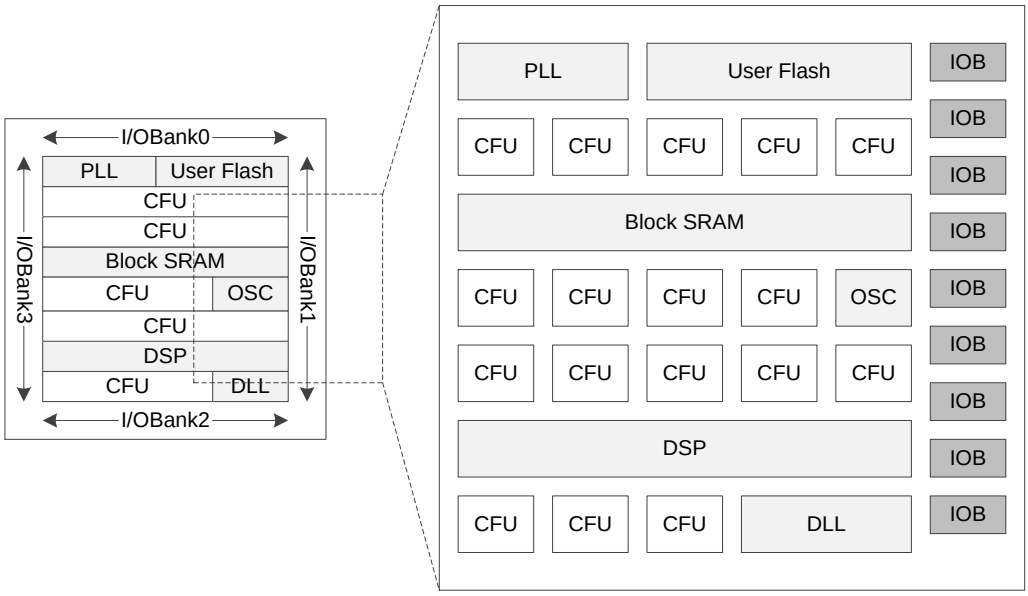


Figure 3-2 is GW1N-4 Architecture Overview. The structures of GW1N-2, GW1N-6, and GW1N-9 are similar to GW1N-4's. The core of GW1N-4 is the array of Configurable Logic Unit (CFU) surrounded by IO blocks. GW1N-4 also provides B-SRAM, DDSP, PLL, DLL, user Flash, and on chip oscillator, and supports Instant-on. See Table 2-1for the detailed information.

Configurable Function Unit (CFU) is the base cell for the array of GW1N series FPGA Products. Devices with different capacities have different numbers of rows and columns. CFU can be configured as LUT4 mode, ALU mode, and Memory mode. Memory mode is supported in GW1N-6 and GW1N. For detailed information, see *3.2CFU*.

The I/O resources in GW1N series FPGA products are arranged around the periphery of the devices in groups referred to as banks, including Bank0, Bank1, Bank2, and Bank3. I/O resources support multiple level standards, and support basic mode, SRD mode, and generic DDR mode. For detailed information, see *3.3IOB*.

The B-SRAM is embedded as row in GW1N series FPGA products. In the FPGA array, each B-SRAM occupies 3 columns of CFU. Each B-SRAM has 18,432 bits (18Kbits) and supports multiple configuration modes and operation modes. For detailed information, see *3.4Block SRAM (B-SRAM)*.

The User Flash is embedded in GW1N series FPGA products. There is no data lost if power off. For detailed information, see *3.5User Flash*.

GW1N-2, GW1N-4, GW1N-6, and GW1N-9 support DSP. DSP blocks are embedded as row in the FPGA array. Each DSP occupies 9 CFU columns. Each DSP block contains 2 Macro, and each Macro contains 2 pre-adders, 2 multipliers with 18 by 18 inputs, and a 3 input ALU54. For detailed information, see *3.6DSP*.

GW1N-2, GW1N-4, GW1N-6, and GW1N-9 provide PLLs and DLLs. GW1N PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty

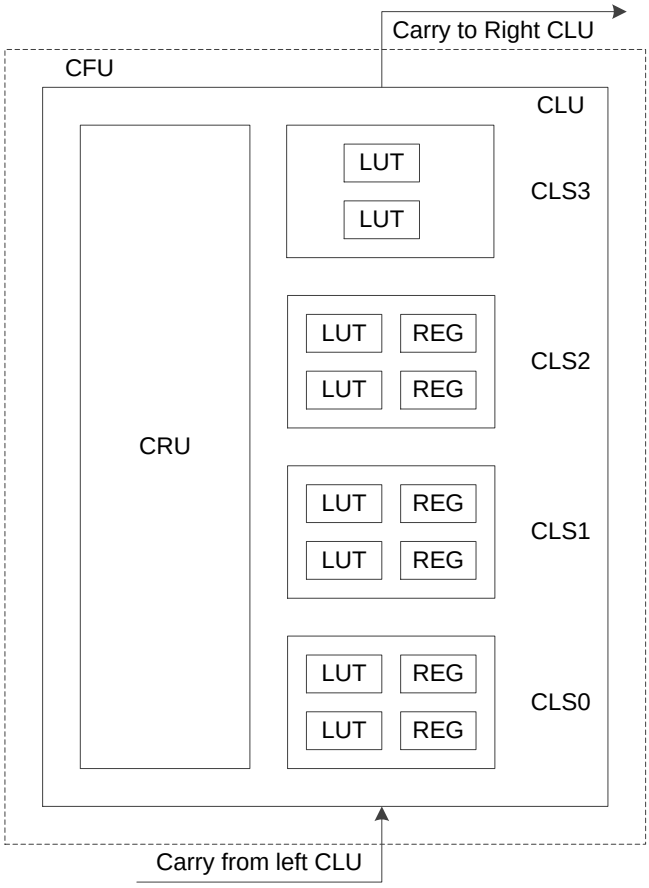
cycle can be adjusted by parameters configuration. There is an internal programmable On Chip Oscillator in each GW1N series FPGA product. On Chip Oscillator supports the clock frequency from 2.5MHz to 125MHz, providing clock for MSPI mode. On Chip Oscillator also provides clock resource for user designs with the clock precision reaching ±5%. For detailed information, see *3.7Clock* and *3.11On Chip Oscillator*.

FPGA provides abundant CRUs, connecting all the resources in FPGA. Routing resources can be generated by Gowin Yunyuan software automatically. Besides that, GW1N series FPGA Products also provide abundant GCLKs, Long Wires (LW), Global Set/Reset (GSR), and programming options, etc. For detailed information, see *3.7Clock*, *3.8Long Wire (LW)*, and *3.9Global Set/Reset (GSR)*.

3.2 CFU

Configurable Function Unit (CFU) is the base cell for the array of GW1N series FPGA Products. Each CFU consists of a Configurable Logic Unit (CLU) and its routing resource Configurable Routing Unit (CRU). In each CLU, there are 4 Configurable Logic Slices (CLS). Each CLS contains Look-Up-Tables (LUT) and registers, as shown in Figure 3-3 below.

Figure 3-3 CFU Strucutre



3.2.1 CLU

CLU supports 3 operation modes: Basic Logic mode, ALU mode, and Memory mode.

- Basic Logic Mode

Each LUT can be configured as one 4 input LUT as it is. Higher input number of LUT can be formed by combining the LUT4 together.

- Each CLS can form one 5 input LUT5.
- 2 CLSs can form one 6 input LUT6.
- 4 CLSs can form one 7 input LUT7.
- 8 CLSs (2 CLUs) can form one 8 input LUT8.

- ALU Mode

Combining with carry chain logic, LUT can be configured as ALU mode

to implement the following functions.

- Adder and subtractor
- Up/Down Counter
- Comparator,including greater-than, less-than, and not-equal-to
- Multiplier

- Memory mode

GW1N-6 and GW1N-9 support memory mode. In this mode, a 16 x 4 S-SRAM or ROM can be constructed by using CLSs.

This SRAM can be initialized during the device configuration stage. The initialization data can be generated in the bit stream file from Gowin Yunyuan software.

In each CLU, there are 4 Configurable Logic Slices (CLS). Each Configurable Logic Slice (CLS) has 2 registers (REG), as shown in Figure 3-4 below.

Figure 3-4 Register in CFU

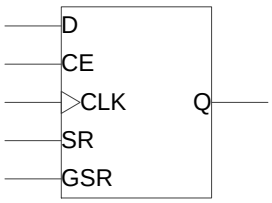


Table 3-1 Register Description in CFU

Signal	I/O	Description
D	I	Data input [1]
CE	I	CLK Enable, can be high or low effective [2]
CLK	I	Clock, can be rising edge or falling edge trigging [2]
SR	I	Set/Reset, can be configured as [2]: ● Synchronized reset ● Synchronized set ● Asynchronous reset ● Asynchronous set ● Non
GSR[3,4]	I	Global Set/Reset, can be configured as[4]: ● Asynchronous reset ● Asynchronous set ● Non
Q	O	Output

Note!

- [1] The source of D can be LUT's output, or the input of CRU, so the register can be used alone when LUTs are in use.
- [2] CE/CLK/SR in CFU are independent.
- [3] In GW1N series FPGA products,GSR has its own dedicated network.
- [4] GSR has higher priority, when both SR and GSR are effective.

3.2.2 CRU

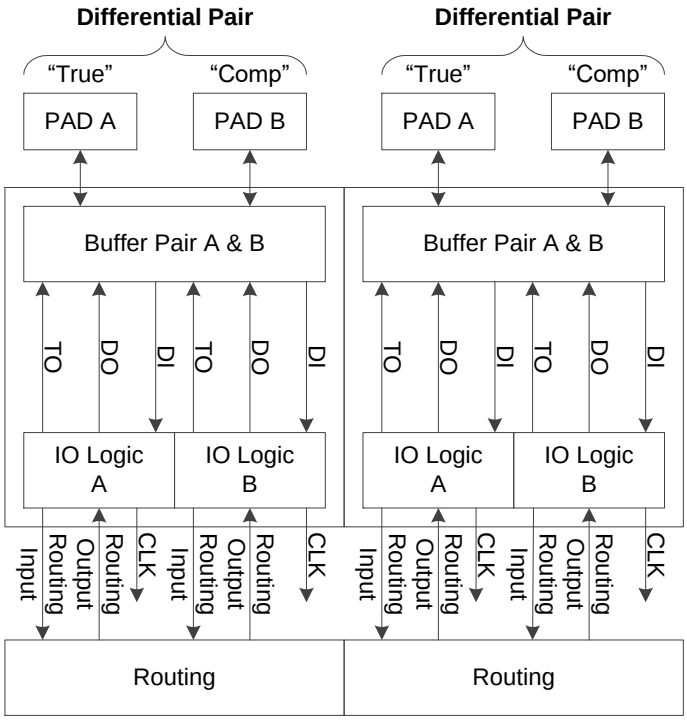
The main functions of CRU are as following:

- Input selection: select input signals for CFU.
- Configurable Routing: connect the input and output of CFUs, including inside CFU, CFU to CFU, and CFU to other functional blocks in FPGA.

3.3 IOB

The IOB in GW1N series FPGA products includes IO Buffer, IO Logic, and its Routing Unit. As shown in Figure 3-5, each IOB connects to 2 Pins (Marked as A and B). They can be used as a differential pair or as 2 single end input/output.

Figure 3-5 IOB StructureView



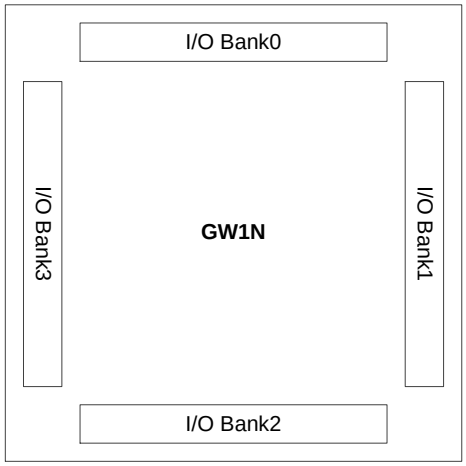
IOB Features:

- V_{CCO} supplies with each Bank
- LVCMOS, PCI, LVTTL, LVDS, SSTL, and HSTL (true LVDS not supported in GW1N-1)
- Input hysteresis option
- Output drive strength option
- Slew Rate option
- Individual Bus Keeper, Weak Pull-up, Weak Pull-down, and Open Drain option
- Hot Socket
- IO Logic supports basic mode, SRD mode, and generic DDR mode

3.3.1 I/O Buffer

There are 4 IO Banks in GW1N series FPGA products, as shown in Figure 3-6. Each Bank has independent IO source V_{CCO}, V_{CCO} can be 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V. In order to support SSTL, HSTL, etc., each bank also provides 1 independent voltage source (VREF) as referenced voltage. User can choose from internal reference voltage of the bank (0.5 x V_{CCO}) or external reference voltage using any IO from the bank.

Figure 3-6 GW1N I/O Bank Distribution



For the V_{CCO} requirements of different IO standards, see Table 3-2 as below.

Table 3-2 Output Standards and Configuration Options

I/O output standard	Single/Differ	Bank V_{CCO} (V)	Driver Strength (mA)
LVTTL33	Single end	3.3	4,8,12,16,24
LVCMOS33	Single end	3.3	4,8,12,16,24
LVCMOS25	Single end	2.5	4,8,12,16
LVCMOS18	Single end	1.8	4,8,12
LVCMOS15	Single end	1.5	4,8
LVCMOS12	Single end	1.2	4,8
SSTL25_I	Single end	2.5	8
SSTL25_II	Single end	2.5	8
SSTL33_I	Single end	3.3	8
SSTL33_II	Single end	3.3	8
SSTL18_I	Single end	1.8	8
SSTL18_II	Single end	1.8	8
SSTL15	Single end	1.5	8
HSTL18_I	Single end	1.8	8
HSTL18_II	Single end	1.8	8
HSTL15_I	Single end	1.5	8
PCI33	Single end	3.3	N/A
LVPECL33	Differential	3.3	16
MVLDS25E	Differential	2.5	16
BLVDS25E	Differential	2.5	16
RSDS25E	Differential	2.5	8
LVDS25E	Differential	2.5	8
LVDS25	Differential	2.5	8
RSDS25E	Differential	2.5	8
SSTL15D	Differential	1.5	8
SSTL25D_I	Differential	2.5	8
SSTL25D_II	Differential	2.5	8
SSTL33D_I	Differential	3.3	8
SSTL33D_II	Differential	3.3	8
SSTL18D_I	Differential	1.8	8
SSTL18D_II	Differential	1.8	8
HSTL18D_I	Differential	1.8	8
HSTL18D_II	Differential	1.8	8
HSTL15D_I	Differential	1.5	8

Table 3-3 Input Standards and Configuration Options

I/O Input Standard	Single/Diff	Bank V_{CCO} (V)	Hysteresis	Need V_{REF}
LVTTL33	Single end	1.5/1.8/2.5/3.3	Yes	No
LVCMOS33	Single end	1.5/1.8/2.5/3.3	Yes	No
LVCMOS25	Single end	1.5/1.8/2.5/3.3	Yes	No
LVCMOS18	Single end	1.5/1.8/2.5/3.3	Yes	No
LVCMOS15	Single end	1.2/1.5/1.8/2.5/3.3	Yes	No
LVCMOS12	Single end	1.2/1.5/1.8/2.5/3.3	Yes	No
SSTL15	Single end	1.5/1.8/2.5/3.3	No	Yes
SSTL25_I	Single end	2.5/3.3	No	Yes
SSTL25_II	Single end	2.5/3.3	No	Yes
SSTL33_I	Single end	3.3	No	Yes
SSTL33_II	Single end	3.3	No	Yes
SSTL18_I	Single end	1.8/2.5/3.3	No	Yes
SSTL18_II	Single end	1.8/2.5/3.3	No	Yes
HSTL18_I	Single end	1.8/2.5/3.3	No	Yes
HSTL18_II	Single end	1.8/2.5/3.3	No	Yes
HSTL15_I	Single end	1.5/1.8/2.5/3.3	No	Yes
PCI33	Single end	3.3	Yes	No
LVDS	Differential	2.5/3.3	No	No
RSDS25	Differential	2.5/3.3	No	No
LVDS25E	Differential	2.5/3.3	No	No
MLVDS25E	Differential	2.5/3.3	No	No
BLVDS25E	Differential	2.5/3.3	No	No
RSDS25E	Differential	2.5/3.3	No	No
LVPECL33	Differential	3.3	No	No
SSTL15D	Differential	1.5/1.8/2.5/3.3	No	No
SSTL25D_I	Differential	2.5/3.3	No	No
SSTL25D_II	Differential	2.5/3.3	No	No
SSTL33D_I	Differential	3.3	No	No
SSTL33D_II	Differential	3.3	No	No
SSTL18D_I	Differential	1.8/2.5/3.3	No	No
SSTL18D_II	Differential	1.8/2.5/3.3	No	No
HSTL18D_I	Differential	1.8/2.5/3.3	No	No
HSTL18D_II	Differential	1.8/2.5/3.3	No	No
HSTL15D_I	Differential	1.5/1.8/2.5/3.3	No	No

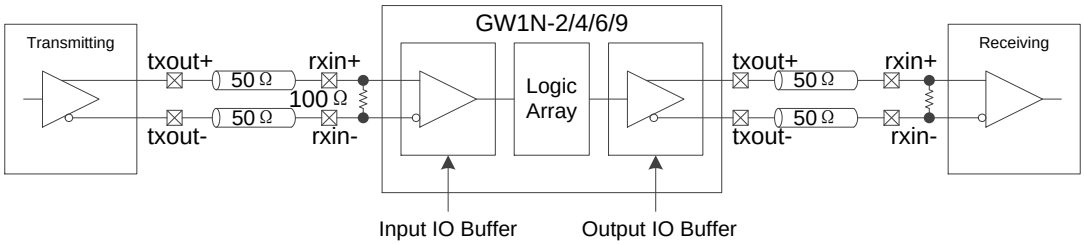
3.3.2 True LVDS Design

BANK1/2/3 in GW1N-2/4/6/9 devices support true LVDS output, but BANK1/2/3 do not support internal 100Ω input differential matched resistence. Bank0 support internal 100Ω input differential matched resistence. BANK0/1/2/3 support LVDS25E, MLVDS25E, BLVDS25E,etc, and for the detailed information about different levels, please refer to *Gowin systemIO User Guide*.

For the detailed information about true LVDS, please refer to *GW1N series FPGA products Pinout.*

True LVDS input IO need external 100Ω terminal resistence for matching. Refer to Figure 3-7.

Figure 3-7 True LVDS Design



For the detailed information about LVDS25E, MLVDS25E, and BLVDS25E on IO terminal matched resistence, please refer to *Gowin systemIO User Guide*.

3.3.3 I/O Logic

Figure 3-8 shows the I/O logic output of GW1N series FPGA products.

Figure 3-8 I/O Logic Output

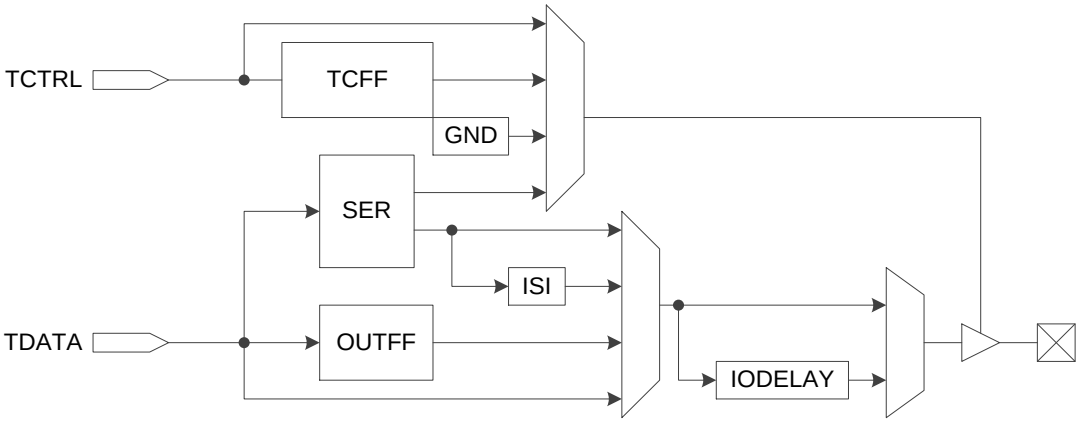
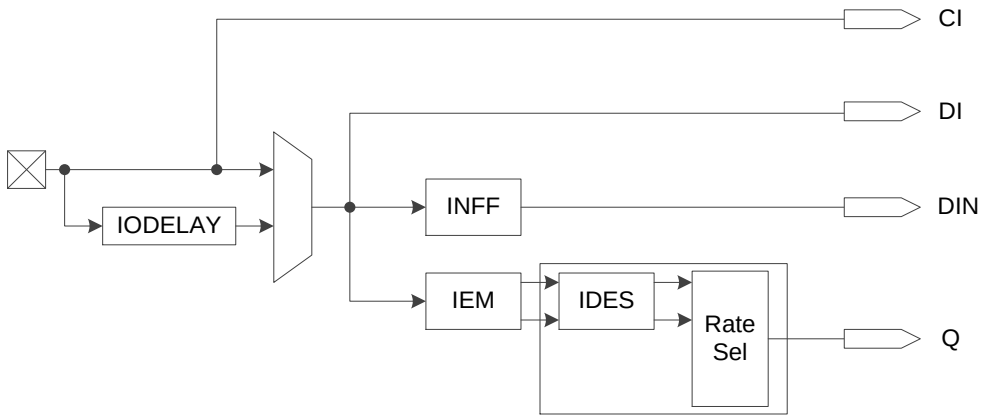


Figure 3-9 shows the I/O logic input of GW1N series FPGA products.

Figure 3-9 I/O Logic Input

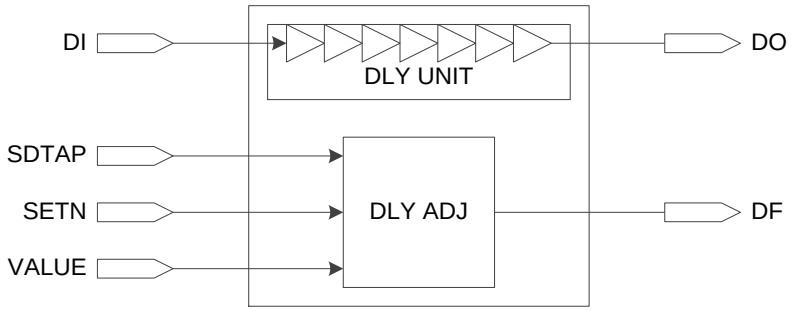


The I/O logic modules description of GW1N series FPGA products is as follows.

IODELAY

Figure 3-10 shows IODELAY. Each I/O of GW1N series FPGA products has an IODELAY cell. The longest delay it can provide is about 128 steps x 25ps = 3200ps.

Figure 3-10 IODELAY



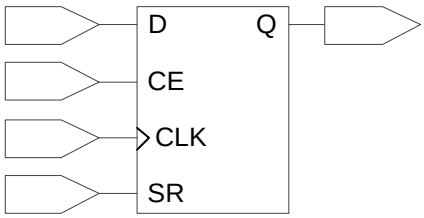
There are 2 ways to control the delay cell:

- Static control: to have fixed delay
- Dynamic control: usually used to sample delay window together with IEM. The IODELAY cannot be used for both input and output at the same time

I/O Register

Figure 3-11 shows I/O register in GW1N series FPGA products. Each IO provides one input register INFF, one output register OUTFF, and a tristate Register TCFF.

Figure 3-11 Register Structure in IO Logic



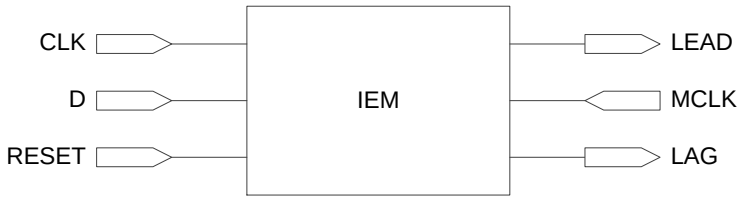
Note!

- CE can be either active-low (0: enable)or active-high (1: enable).
- CLK can be either rising edge trigger or falling edge trigger.
- SR can be either synchronous/asynchronous SET or RESET or disable.
- The register can be programmed as register or latch.

IEM

IEM is for sampling clock edge and is used in generic DDR mode.Figure 3-12 shows the IEM structure.

Figure 3-12 IEM Structure



De-serializer DES and Clock Domain Transfer

GW1N series FPGA products provide a simple de-serializer DES for each input IO to allow support of the advanced IO protocols.

Serializer SER

GW1N series FPGA products provide a simple Serializer SER for each output IO to allow support of the advanced IO protocols.

3.3.4 I/O Logic Modes

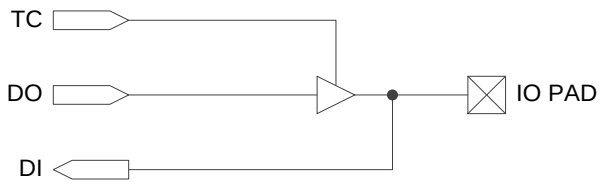
IO Logic in GW1N series FPGA products supports several operations. In each of the operation, the IO (or IO differential pair) can be configured as output, input, and INOUT or tristate output (Output signal with tristate control).

Not all the device pins support IO logic. GW1N-1 pins IOL6 (A,B,C….J) and IOR6 (A,B,C….J) do not support IO logic.GW1N-2 and GW1N-4 pins IOL10 (A,B,C….J) and IOR10 (A,B,C….J) do not support IO logic.

Basic Mode

In basic mode, the IO Logic is as shown in Figure 3-13 below, and the signal TC, DO, and DI can connect to the internal cores directly through CRU.

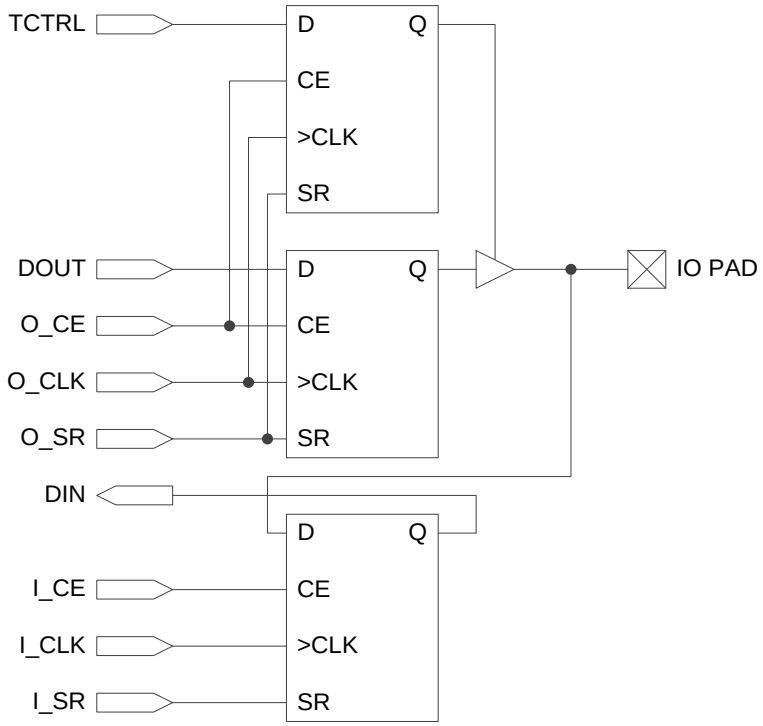
Figure 3-13 IO Logic in Basic Mode



SDR Mode

Compared with the basic mode, SDR utilizes IO register, as shown in Figure 3-14, which can effectively improve IO timing.

Figure 3-14 IO Logic in SDR Mode



Note!

- CLK enable O_CE and I_CE can be configured as active-high or active-low.
- O_CLK and I_CLK can be either rising edge trigger or falling edge trigger.
- Local set/reset signal O_SR and I_SR can be either Synchronized reset,Synchronized set, Asynchronous reset, Asynchronous set, or no-function.
- I/O in SDR mode can be configured as basic register or latch.

Generic DDR Mode

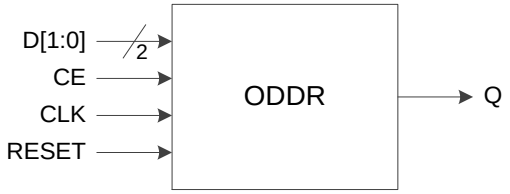
In generic DDR mode, GW1N series FPGA products support higher speed IO protocols.

Figure 3-15 shows generic DDR input, with the speed ratio of internal logic to PAD 1:2.

Figure 3-15 I/O Logic in DDR Input Mode

Figure 3-16 shows generic DDR output, with the speed ratio of PAD to FPGA internal logic 2:1.

Figure 3-16 I/O Logic in DDR Output Mode



IDES4

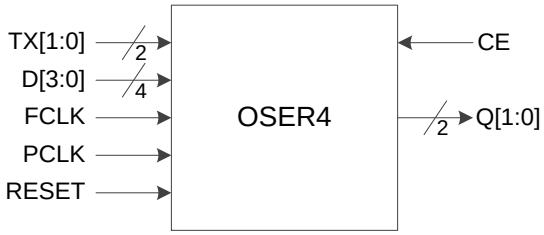
In IDES4 mode, higher speed signals can be supported. The frequency of input signal (D) and the frequency of output signal Q to the core has a ratio of 4:1.

Figure 3-17 IO Logic in IDES4 Mode

OSER4 Mode

In IDES4 mode, higher speed signals can be supported. The frequency of input signal (D) and the signal Q which is transferred to Pin has a ratio of 1:4.

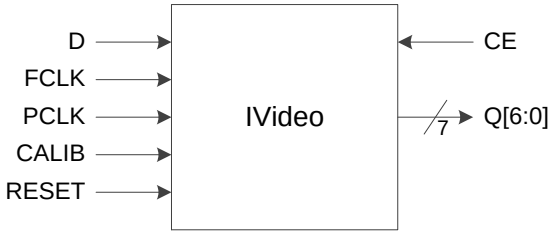
Figure 3-18 IO Logic in OSER4 Mode



IVideo Mode

In IVideo mode, higher speed signals can be supported. The signal (D) frequency at the input of this block vs the signal Q which is transferred to core has a ratio of 7:1.

Figure 3-19 IO Logic in IVideo Mode



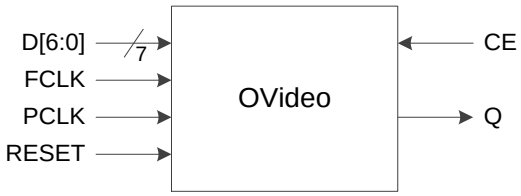
Note!

IVideo and IDES8/10 will occupy the neighboring IO Logic. If the IO Logic of a pin is occupied, the pin can be programmed in SDR or Basic mode.

OVideo Mode

In Ovideo mode, higher speed signals can be supported. The signal (D) frequency at the input of this block vs the signal Q which is transferred to Pin has a ratio of 1:7.

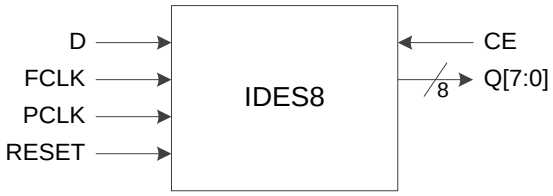
Figure 3-20 IO Logic in OVideo Mode



IDES8 Mode

In IDES8 mode, higher speed signals can be supported. The signal (D) frequency at the input of this block vs the signal Q which is transferred to core has a ratio of 8:1.

Figure 3-21 IO Logic in IDES8 Mode



OSER8 Mode

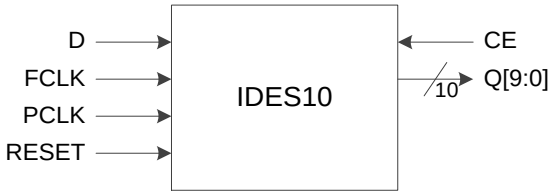
In OSER8 mode, higher speed signals can be supported. The signal (D) frequency at the input of this block vs the signal Q which is transferred to Pin has a ratio of 1:8.

Figure 3-22 IO Logic in OSER8 Mode

IDES10 Mode

In IDES10 mode, higher speed signals can be supported. The signal (D) frequency at the input of this block vs the signal Q which is transferred to core has a ratio of 10:1.

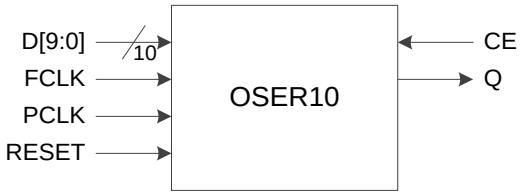
Figure 3-23 IO Logic in IDES10 Mode



OSER10 Mode

In OSER10 mode, higher speed signals can be supported. The signal (D) frequency at the input of this block vs the signal Q which is transferred to Pin has a ratio of 1:10.

Figure 3-24 IO Logic in OSER10 Mode



3.4 Block SRAM (B-SRAM)

3.4.1 Introduction

GW1N series FPGA products provide SRAM. The Block SRAM is embedded as row in the FPGA array. Its called B-SRAM which is different from S-SRAM (Shadow SRAM). In the FPGA array, each B-SRAM occupies 3 columns of CFU.Each B-SRAM has 18,432 bits (18Kbits). There are 5 operation modes: Single Port, Dual Port, Semi Dual Port, ROM, and FIFO.

B-SRAM features:

- Max.18,432 bits per B-SRAM

- B-SRAM itself can run at 190MHz at max (typical, Read-before-write is 110MHz)
- Single Port
- Dual Port
- Semi Dual Port
- Parity Bits
- ROM
- Data width 1 to 36 bits
- Mixed Clock Mode
- Mixed Data Width Mode
- Enable Byte operation for double byte or above
- Asynchronous reset, Synchronous reset
- Normal Read and Write Mode
- Read-before-write Mode
- Write-through Mode

Table 3-4 B-SRAM Signals

Port Name	I/O	Description
DIA	I	Port A data input
DIB	I	Port B data input
ADA	I	Port A Address
ADB	I	Port B Address
CEA	I	Clock Enable, Port A
CEB	I	Clock Enable, Port B
RESETA	I	Register Reset, Port A
RESETB	I	Register Reset, Port B
WREA	I	Read/Write Enable, Port A
WREB	I	Read/Write Enable, PortB
BLKSEL	I	Block Select
CLKA	I	Read/Write Cycle Clock for Port A input registers
CLKB	I	Read/Write Cycle Clock for Port B input registers
OCEA	I	Clock enable for Port A output registers
OCEB	I	Clock enable for Port B output registers
DOA	O	Port A data output
DOB	O	Port B data output

3.4.2 Modes Configuration

The B-SRAM mode in GW1N series FPGA products supports different data bus widths. See Table 3-5.

Table 3-5 Memory Size Configuration

Single Port	Dual Port	Semi Dual Port	Read Only
16K x 1	16K x 1	16K x 1	16K x 1
8K x 2	8K x 2	8K x 2	8K x 2
4K x 4	4K x 4	4K x 4	4K x 4
2K x 8	2K x 8	2K x 8	2K x 8
1K x 16	1K x 16	1K x 16	1K x 16
512 x 32	-	512 x 32	512 x 32
2K x 9	2K x 9	2K x 9	2K x 9
1K x 18	1K x 18	1K x 18	1K x 18
512 x 36	-	512 x 36	512 x 36

3.4.3 Mixed Data Bus Width Configuration

B-SRAM in GW1N series FPGA products supports mixed data bus width operation. In dual port and semi-dual port modes, the data bus width for read and write can be different. For available configuration, please see Table 3-6 and Table 3-7 below.

Table 3-6 Dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port						
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	2K x 9	1K x 18
16K x 1	*	*	*	*	*		
8K x 2	*	*	*	*	*		
4K x 4	*	*	*	*	*		
2K x 8	*	*	*	*	*		
1K x 16	*	*	*	*	*		
2K x 9						*	*
1K x 18						*	*

Note!

“*”means the modes supported.

Table 3-7 Semi Dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port								
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	512 x 32	2K x 9	1K x 18	512 x 36
16K x 1	*	*	*	*	*	*			
8K x 2	*	*	*	*	*	*			
4K x 4	*	*	*	*	*	*			
2K x 8	*	*	*	*	*	*			
1K x 16	*	*	*	*	*	*			
512 x 32	*	*	*	*	*	*			
2K x 9							*	*	*
1K x 18							*	*	*

Note!

"*"means the modes supported.

3.4.4 Byte-enable

B-SRAM in GW1N series FPGA products support byte-enable. For a data longer than a Byte, the additional bits can be blocked, and only the selected portion is written into. The blocked bits will be kept for future operation. Read/Write enable ports (WREA, WREB), and byte-enable parameter options can be used to control B-SRAM write operation.

3.4.5 Parity Bit

There are parity bits in B-SRAM. The 9^{th} bit in each byte can be used as parity bit or for data storage. However, the parity operation is not supported yet.

3.4.6 Synchronous Operation

- All the input registers of B-SRAM support synchronous write.
- The output registers can be used as pipeline register to improve design performance.
- The output registers are bypass-able.

3.4.7 Power up Conditions

B-SRAM initialization is supported when powering up. During the power up process, B-SRAM is in standby mode, and all the data outputs are"0". This also applies to ROM mode.

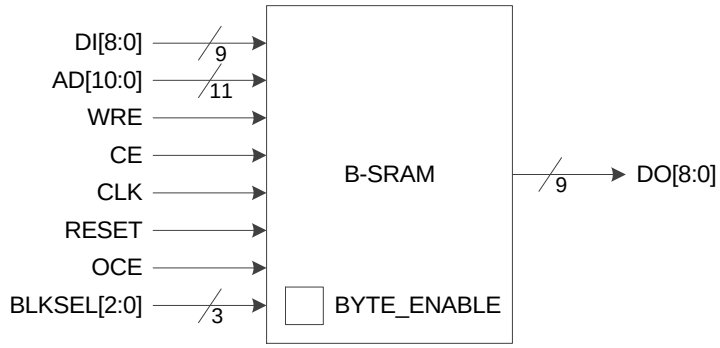
3.4.8 Operation Modes

The input registers of B-SRAM can be used for synchronous write. The output registers can be used as pipeline register to improve design performance. In dual port mode, B-SRAM's 2 ports can be operated totally independently. Port A and Port B have their own clock and write enable, so both ports can write and read independently from each other.

Single Port Mode

In single port mode, as shown below, B-SRAM can write to or read from one port at one clock edge. During the write operation, the data can show up at the output of SRAM. Normal write mode and Write-through mode can be supported. When the output register is bypassed, the new data will show at the same write clock rising edge. For the single port 2K x 9bit block memory, see Figure 3-25 below.

Figure 3-25 Single Port Block Memory



The table below shows all the configuration options for single port mode:

Table 3-8 Single Port Block Memory Configuration

Primitive	Configuration	RAM bits	Port Mode	Memory Depth	Data Depth
SP	B-SRAM_16K_S1	16K	16K x 1	16,384	1
	B-SRAM_8K_S2	16K	8K x 2	8,192	2
	B-SRAM_4K_S4	16K	4K x 4	4,096	4
	B-SRAM_2K_S8	16K	2K x 8	2,048	8
	B-SRAM_1K_S16	16K	1K x 16	1,024	16
	B-SRAM_512_S32	16K	512 x 32	512	32
SPX9	B-SRAM_2K_S9	18K	2K x 9	2,048	9
	B-SRAM_1K_S18	18K	1K x 18	1,024	18
	B-SRAM_512_S36	18K	512 x 36	512	36

Dual Port Mode

B-SRAM support Dual Port mode, as shown in Figure 3-26. The operations are:

- 2 independent read
- 2 independent write
- An independent read and an independent write at different clock frequency

Figure 3-26 Dual Port Block Memory

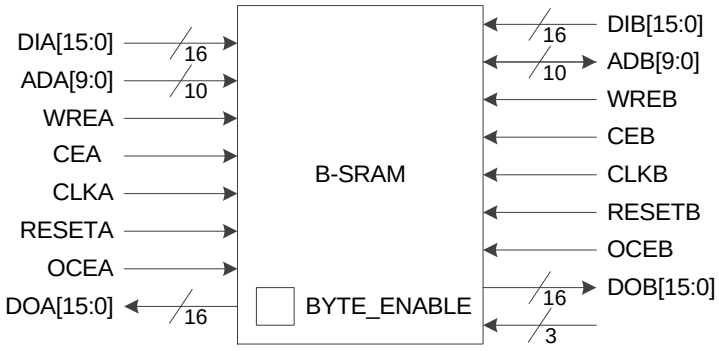


Table 3-9 shows all the configuration options for dual port mode.

Table 3-9 Dual Port Block Memory Configuration

Primitive	Configuration	RAM Bits	Port Mode	RAM Width	Data Width
DP	B-SRAM_16K_D1	16K	16K x 1	16384	1
	B-SRAM_8K_D2	16K	8K x 2	8192	2
	B-SRAM_4K_D4	16K	4K x 4	4096	4
	B-SRAM_2K_D8	16K	2K x 8	2048	8
	B-SRAM_1K_D16	16K	1K x 16	1024	16
DPX9	B-SRAM_2K_D9	18K	2K x 9	2048	9
	B-SRAM_1K_D18	18K	1K x 18	1024	18

Semi Dual Port Mode

Figure 3-27 shows semi Dual Port mode. It supports read and write at same time on different ports. We cannot write and read at same port at same time.

Figure 3-27 Semi Dual Port Block Memory

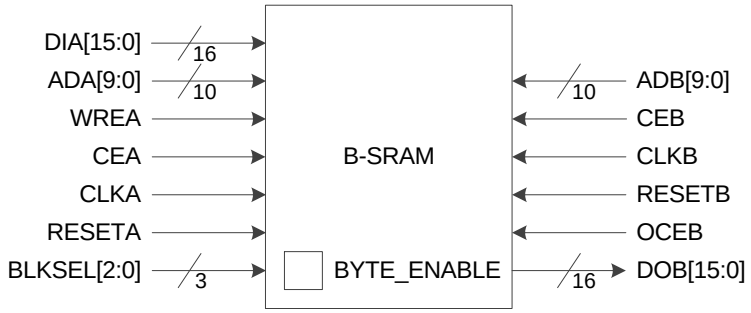


Table 3-10 shows all the configuration options for semi dual port mode:

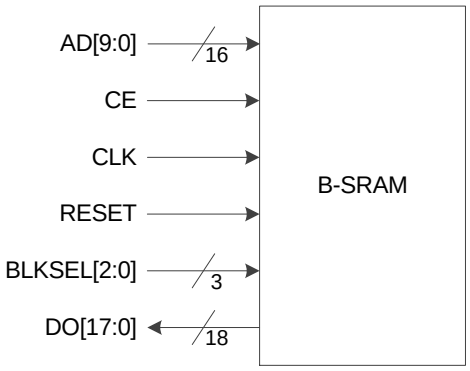
Table 3-10 Semi Dual Port Memory Configuration

Primitive	Configuration	RAM bits	Port Mode	Memory Depth	Data Width
SDP	B-SRAM_16K_SD1	16K	16K x 1	16,384	1
	B-SRAM_8K_SD2	16K	8K x 2	8,192	2
	B-SRAM_4K_SD4	16K	4K x 4	4,096	4
	B-SRAM_2K_SD8	16K	2K x 8	2,048	8
	B-SRAM_1K_SD16	16K	1K x 16	1,024	16
	B-SRAM_512_SD32	16K	512 x 32	512	32
SDPX9	B-SRAM_2K_SD9	18K	2K x 9	2,048	9
	B-SRAM_1K_SD18	18K	1K x 18	1,024	18
	B-SRAM_512_SD36	18K	512 x 36	512	36

ROM Mode

B-SRAM can be configured as ROM, as shown in Figure 3-28. The ROM can be initialized during device configuration stage, and the ROM data need to be provided in the initialization file.

Figure 3-28 ROM Block Memory



Each B-SRAM can be configured as one 16Kbits ROM. Table 3-11 lists all the configuration options for ROM mode.

Table 3-11 Block ROM Configuration

Primitive	Configuration	RAM bits	Port Mode	Memory Depth	Data Width
ROM	B-SRAM_16K_O1	16K	16K x 1	16,384	1
	B-SRAM_8K_O2	16K	8K x 2	8,192	2
	B-SRAM_4K_O4	16K	4K x 4	4,096	4
	B-SRAM_2K_O8	16K	2K x 8	2,048	8
	B-SRAM_1K_O16	16K	1K x 16	1,024	16
	B-SRAM_512_O32	16K	512 x 32	512	32
ROMX9	B-SRAM_2K_O9	18K	2K x 9	2,048	9
	B-SRAM_1K_O18	18K	1K x 18	1,024	18
	B-SRAM_512_O36	18K	512 x 36	512	36

Note!

In ROM mode, the signal RESET can only reset the input and output registers. It cannot clear the ROM content.

3.4.9 B-SRAM Operation Modes

B-SRAM supports 5 different operations, including 2 read operations (Bypass Mode and Pipeline Read Mode) and 3 write operations (Normal Write Mode, Write-through Mode, and Read-before-write Mode).

Read Mode

Read data from B-SRAM via output registers or without using the registers.

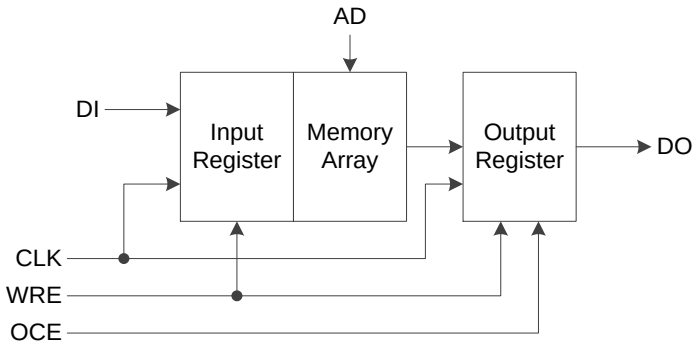
Pipeline Mode

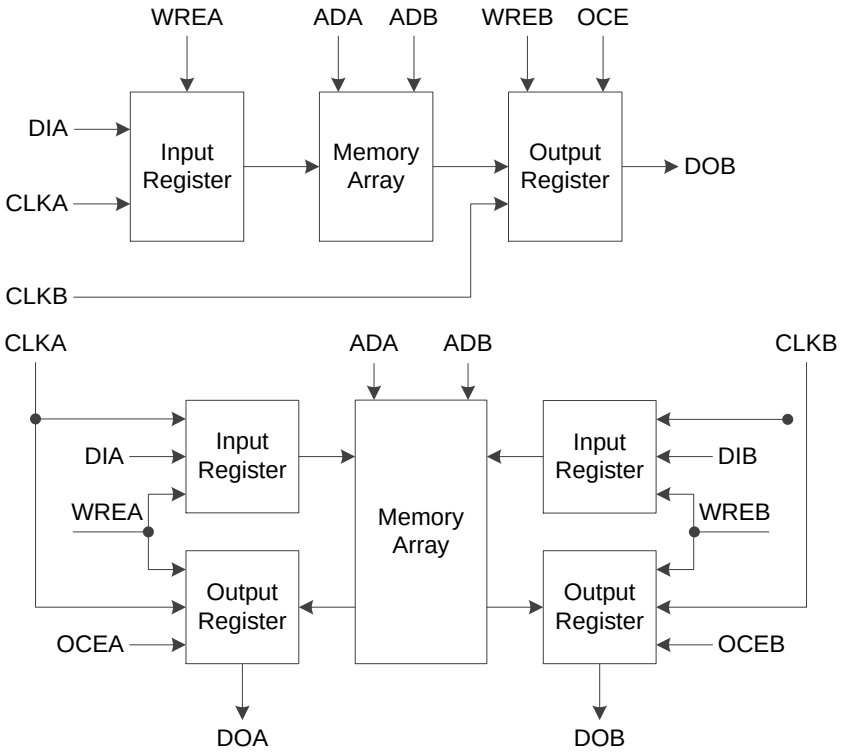
While writing in the B-SRAM, the output register and pipeline register are also being written. The data bus can be up to 36 bits in this mode.

Bypass Mode

The output register and pipeline register are not used. The data output is the output of Memory Array.

Figure 3-29 Pipeline Mode in Single Port, Dual Port and Semi Dual Port





Write Modes

Normal Write Mode

Write data to one port, and the output data of this port do not change. The data written in will not show up at the read port.

Write-through Mode

In the mode, write data to one port, and the data written in will also show up at the output of this port.

Read-before-write Mode

In this mode, write data to one port, and the data written in will be stored in the memory according to the address. The original data in this address will show up at the output of this port.

3.4.10 Clock Operations

Table 3-12 lists clock operations in different B-SRAM modes:

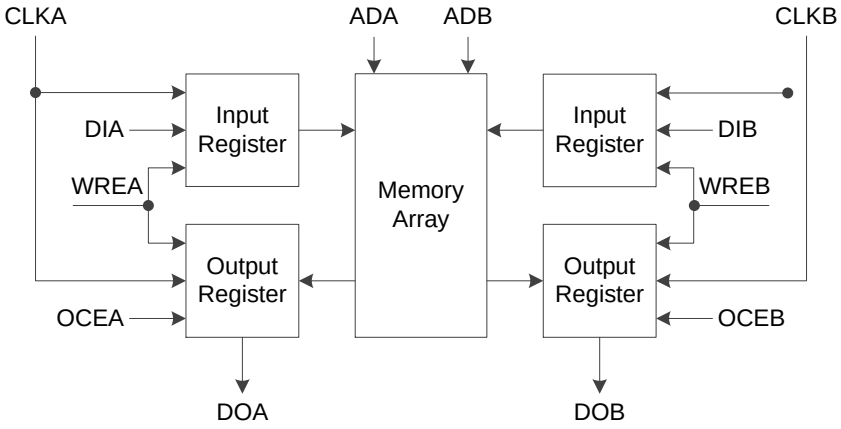
Table 3-12 Clock Operations in Different B-SRAM Modes

Clock	Dual Port Mode	Semi Dual Port Mode	Single Port Mode
Independent	Yes	No	No
Read/Write	Yes	Yes	No
Single Port	No	No	Yes

Independent Clock

Figure 3-30 shows the independent clocks in dual port mode with each port with one clock. CLKA controls all the registers at Port A; CLKB controls all the registers at Port B.

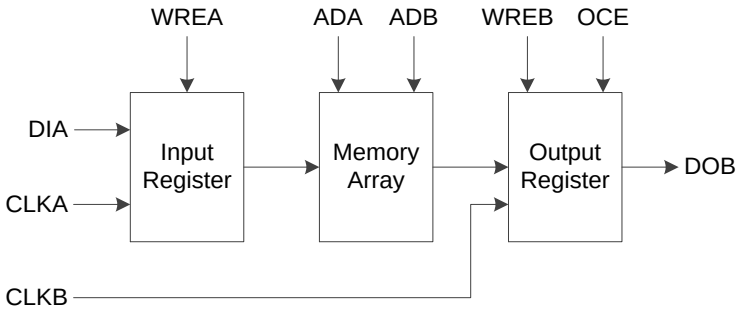
Figure 3-30 Independent Clock Mode



Read/Write Clock Operation

Figure 3-31 shows the read/write clock operations in semi dual port mode with each port one clock. Write clock (CLKA)controls Port A data inputs, write address and read/write enable signals. Read clock (CLKB)controls Port B data output, read address, and read enable signals.

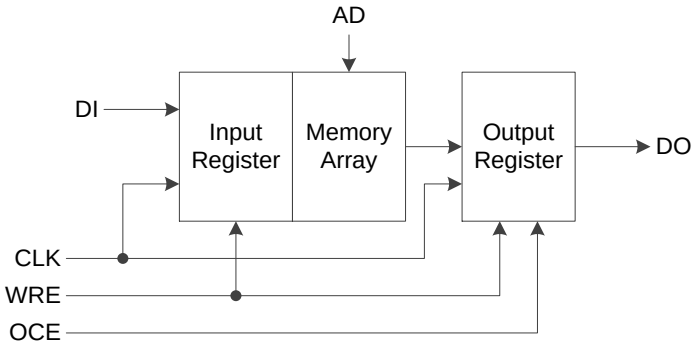
Figure 3-31 Read/Write Clock Mode



Single Port Clock Mode

Figure 3-32 shows the clock operation in single port mode.

Figure 3-32 Single Port Clock Mode



3.5 User Flash

3.5.1 Introduction

GW1N series FPGA products support User Flash. The features are as

following:

- 10,000 write cycles
- Greater than10 years Data Retention at +85℃
- Page Erase Capability: 2,048 bytes per page
- Fast Page Erasure/Word Programming Operation
- Working clock frequency:no less than 40MHz
- Word Programming Time:≤16μs
- Page Erasure Time:≤120ms
- Current
  - Read current/duration:2.19mA/25ns (V_{CC}) & 0.5mA/25ns (V_{CCX}) (MAX)
  - Programming/erasure operation:12/12mA (MAX)

3.5.2 User Flash Ports

Figure 3-33 shows GW1N-1 user flash ports:

Figure 3-33 GW1N-1 User Flash Ports

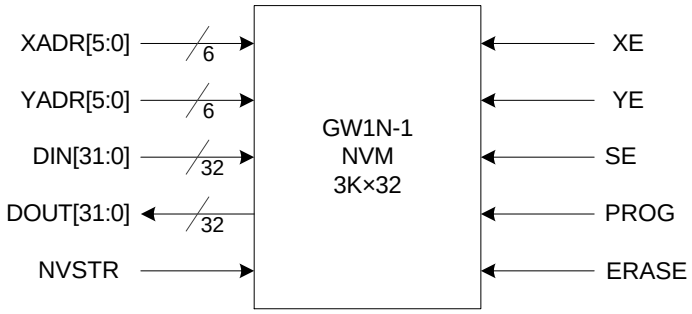


Table 3-13 Pin Description

Pin name[1]	I/O	Description
XADR[5:0][2]	I	X address bus, used to select one row within a page of main memory block.
YADR[5:0][2]	I	Y address bus, used to select one column within a row of memory block.
DIN[31:0]	I	Data input bus.
DOUT[31:0]	O	Data output bus.
XE[2]	I	X address enable, all rows are disabled when XE=0.
YE[2]	I	Y address enable, all columns are disabled when YE=0.
SE[2]	I	Sense amplifier enable, active-high.
ERASE	I	Erase port, active-high.
PROG	I	Programme port, active-high.
NVSTR	I	Flash data storage port, active-high.

Note!

- [1] Port names of Control, address,and data signals.
- [2] Only when XE=YE=V_{CC} and SE meets pulse timing (Tpws, Tnws) requirement, read operation is valid, and read-out data is based on information of XADR[5:0] and YADR[5:0].

3.5.3 User Flash Mode Truth Table

User Mode

Table 3-14 User Mode Truth Table

Mode	XE	YE	SE	PROG	ERASE	NVSTR
Read	H	H	H	L	L	L
Program	H	H	L	H	L	H
Page Erase	H	L	L	L	H	H

Note!

"H" and "L" means high level or low level of V_{CC}.

3.6 DSP

3.6.1 Introduction

GW1N series FPGA products (except GW1N-1) have rich DSP modules. Gowin DSP solutions can meet user demands for high performance digital signal processing design, such as FIR, FFT, etc. DSP blocks have the advantages of stable timing performance, high-usage, and low-power.

DSP blocks are embedded as row in the FPGA array. Each DSP occupies 9 CFU columns. Each DSP block contains 2 Macro, and each Macro contains 2 pre-adders, 2 multipliers with 18 by 18 inputs, and a 3 input ALU.

DSP offers the following functions:

- Multiplier with 3 width, signed and unsigned data: 9-bit, 18-bit, 36-bit
- Multiplier and Accumulator (MAC)
- Multipliers cascading to support wider data
- Barrel Shifter
- Adaptive filtering through signal feedback
- Computing with options of rounding to positive number or prime number
- Bypass options for all stage registers

Macro

Figure 3-34 shows the structure of one Macro:

Figure 3-34 DSP Macro

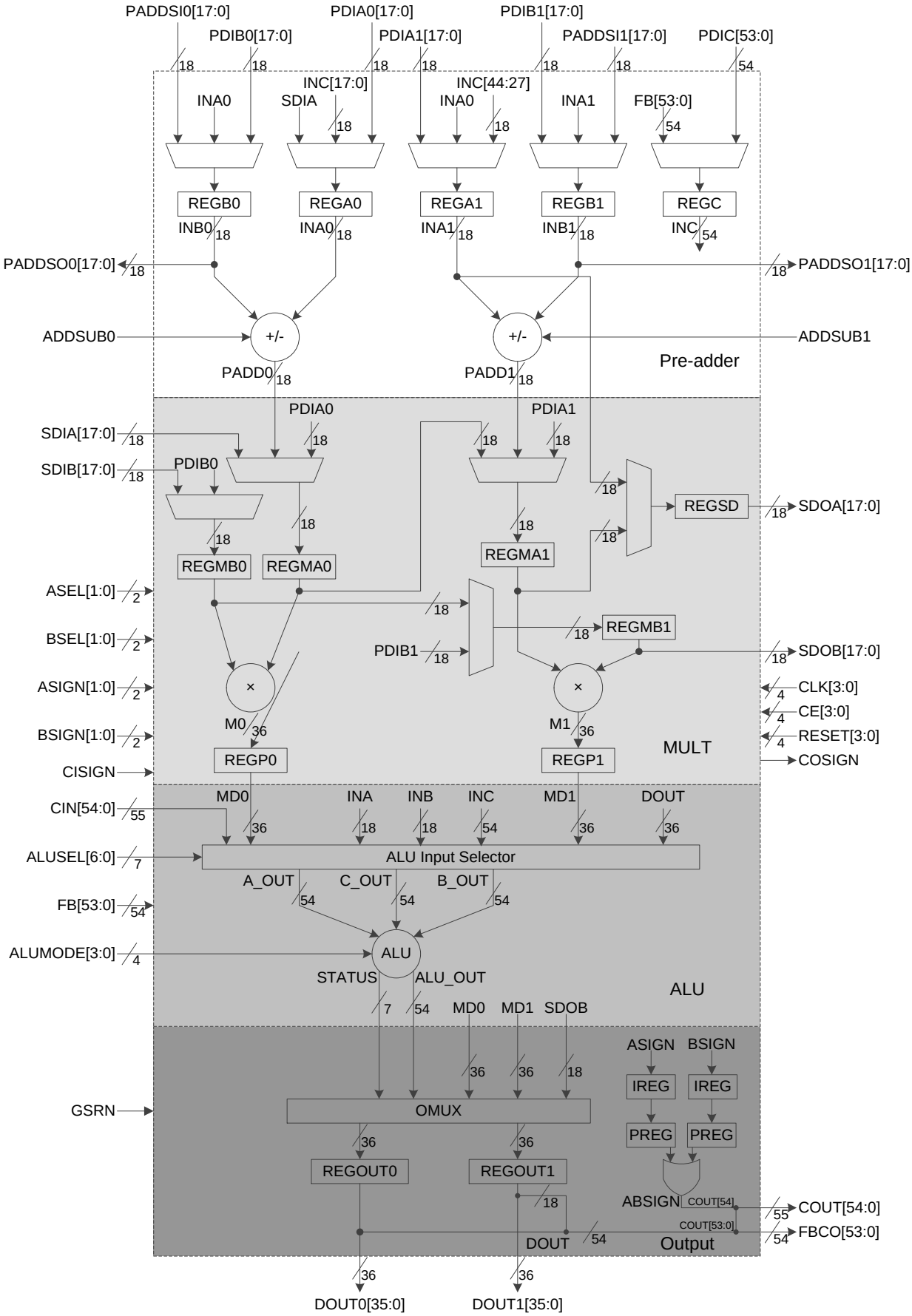


Table 3-15 decribes Micro signal function:

Table 3-15 DSP Ports Description

Port Name	I/O	Description
PDIA0[17:0]	I	parallel data input port A0
PDIB0[17:0]	I	parallel data input port B0
PDIA1[17:0]	I	parallel data input port A1
PDIB1[17:0]	I	parallel data input port B1
PDIC[53:0]	I	parallel data input port C
SDIA[17:0]	I	shift data input port A
SDIB[17:0]	I	shift data input port B
PADDSI0[17:0]	I	Pre-adder shift data input port
PADDSI1[17:0]	I	Pre-adder shift data input port
CIN[54:0]	I	ALU input from previous DSP block
FB[53:0]	I	FBCO feedback from next DSP block, used for high speed output DDR interface implementation
ASEL[1:0]	I	Source selector for Multiplier input A or for pre-adder input A
BSEL[1:0]	I	Source selector for Multiplier input B
ASIGN [1:0]	I	Sign bit for input A, MSB for port A1 and LSB for port A0
BSIGN [1:0]	I	Sign bit for input B, high for port B1 and low for port B0
CISIGN	I	Sign bit from previous DSP block
ADDSUB0	I	pre-adder control signal, used for add/subtract selection
ADDSUB1	I	pre-adder control signal, used for add/subtract selection
ALUSEL[6:0]	I	ALU control signal, ALU input selector
ALUMODE[3:0]	I	ALU control signal, ALU operation configuration
CLK[3:0]	I	clock input
CE[3:0]	I	clock enable
RESET[3:0]	I	Reset input , synchronous or asynchronous
GSRN	Global Input	Global reset, reset all registers
SDOA[17:0]	O	shift data output port A
SDOB[17:0]	O	shift data output port B
PADDSO0[17:0]	O	pre-adder shift data output
PADDSO1[17:0]	O	pre-adder shift data output
DOUT0[35:0]	O	DSP output data LSB 36
DOUT1[35:0]	O	DSP output data MSB 36
COUT[54:0]	O	ALU output to next DSP block, the highest bit is sign extended
FBCO[53:0]	O	DSP output, used to feedback to the previous DSP block. Used for high speed output interface implementation
COSIGN	O	used for the next DSP signed output

Pre-adder

There are two 18 bit adder units in pre-adder block. Pre-Adder supports 18 bit input PDIA, PDIB, PDIC, or SDIA. One set of register chain can be used for data shifting and data input ahead, which improves the computation performance. These registers can be bypassed, so the PDI_A and PDI_B can directly feed the Multiplier.

MULT (Multiplier)

Multipliers are follow the Pre-adder.

Each Macro contains the following operations:

- One 18 x 36 multiplier
- Two 18 x 18 multipliers
- Four 9 x 9 multipliers

Two adjacent DSP macros can form a 36 x 36 multiplier.

ALU

Each Macro has one 54 bits ALU54, which can further enhance MULT's functions. The features are as following:

- Pipeline registers
- Dynamically occupy ALU
- Dedicate output register
- Supports Time division multiplexing (TDM)

ALU54 Status

Compare ALU54 output DOUT with the preset constant, which can be MD0, MD1, MD, or PDIC. Only one constant can be used at a given time.

DOUT can be compared with MD0, MD1, or PDIC Statically, and compared with PDIC dynamically. PDIC can be set to any data or signal.

For the detailed information, see Table 3-16 and Table 3-17.

Table 3-16 Input Status

Input status	Definition
DOUT	54-bit ALU results
MD0	54-bit constant pattern, used to detect DOUT: all “0” or all “1”
MD1	54-bit constant pattern 1 , used to detect other patterns of DOUT
MD2	54-bit constant pattern 2 , used to detect other patterns of DOUT
PDIC	Used for dynamical pattern matching

Table 3-17 Output Status

Output Status	Definition	Status Values
CMPZ	comparison of DOUT with 0	1: DOUT = 0
MCMPZ	comparison of masked DOUT with 0	1: masked DOUT=0
MCMPO	comparison of masked DOUT with 1	1: masked DOUT=1
MDCMP	compare DOUT with mask to pattern	1: DOUT is consistant with MC_INIT
MDNCMP	Inverse of MDCMP	1: DOUT is not consistant with MC_INIT
OVER	ALU output overflow	1: DOUT overflow
UNDER	ALU output underflow	1: DOUT underflow

MUX and DSP_OUT_REGS

MUX and DSP_OUT_REGS are made up with multiplexer and register. The 8 bit status of ALU can be output to MUX and DSP_OUT_REG. Then they will show up at DSP_OUT1 [25:18].

3.6.2 DSP Operations

Based on ALUSEL [6:0] and ALUMODE [3:0], DSP can be configured as different operation modes:

- Multiplier
- Accumulator
- Sum
- Sum of sum
- Cascade sum

Control signal can be further divided as following:

- AMUXSEL[1:0]
- BMUXSEL[1:0]
- CMUXSEL[2:0]
- OPPRE[1:0]
- OP[3:0]

3.7 Clock

The clock resources are critical for high performance applications in FPGA. GW1N series FPGA products provide the global clock network

(GCLK) which connects to all the registers directly. Besides the global clock network, GW1N series FPGA products provide high speed clock HCLK. Also GW1N-2, GW1N-4, GW1N-6, and GW1N-9 provide PLL, DLL, etc.

3.7.1 Global Clock

GCLK is distributed in GW1N-1 as two quadrants, L and R. Each quadrant provides 8 GCLKs.The optional clock resources of GCLK can be pins or CRU. Selecting clock from pins can have better timing.

Figure 3-35 GW1N-1 Clock Resources

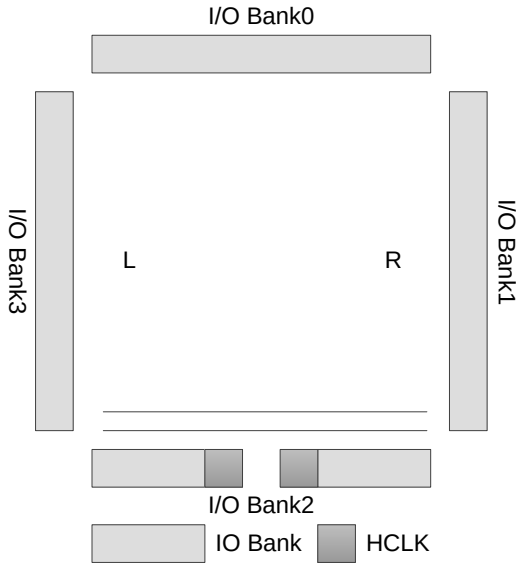


Figure 3-36 GW1N-2/4 Clock Resources

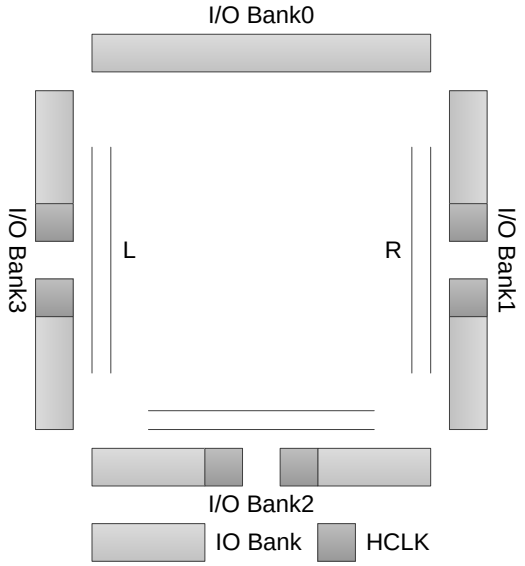
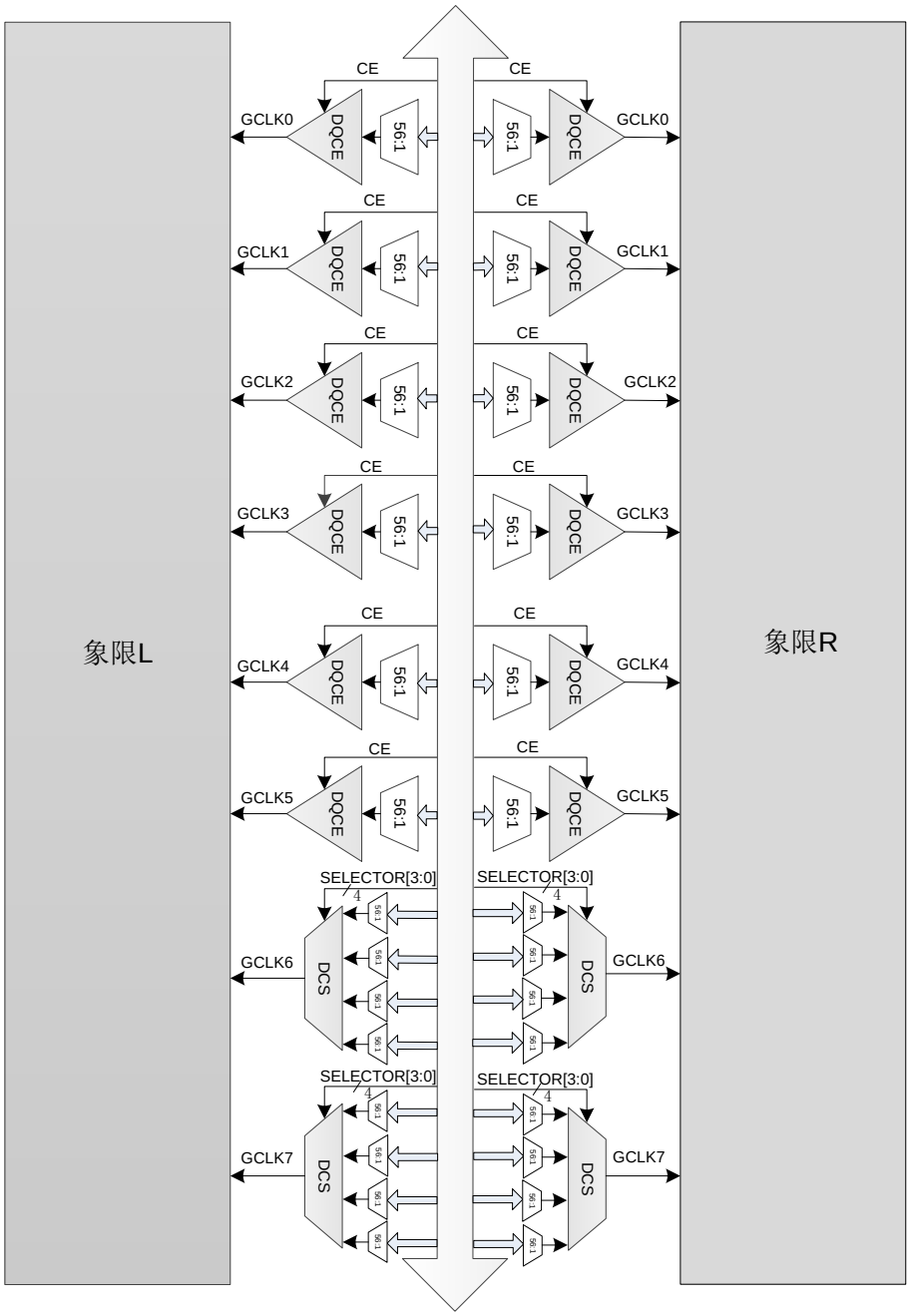
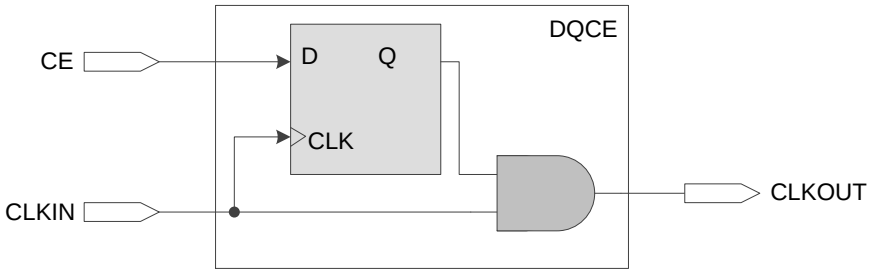


Figure 3-37 GCLK Quadrant Distribution



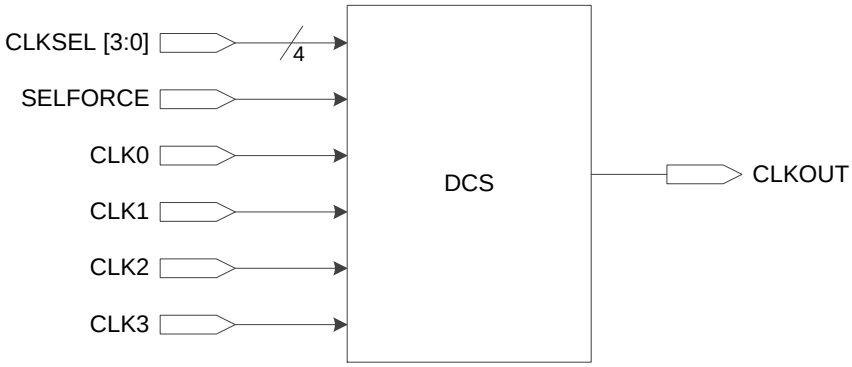
GCLK0~GCLK5 can be dynamically turned on or off by DQCE (Dynamic Quadrant Clock Enable). When GCLK0~GCLK5 in the Quadrant is off, all the logic driven by it will not toggle, therefore, lower power can be achieved.

Figure 3-38 DQCE Concept



GCLK6~GCLK7 of each quadrant is controlled by DCS (Dynamic Clock Selector), as shown in Figure 3-39. Select dynamically between CLK0~CLK3 by CRU, and output a glitch free clock.

Figure 3-39 DCS Concept

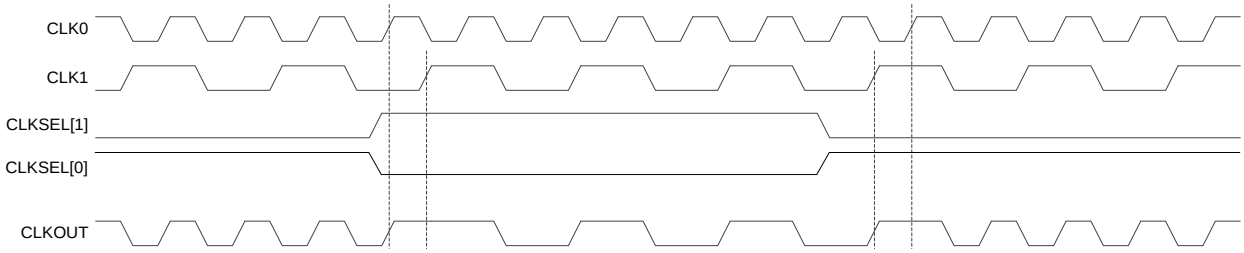


DCS can be configured in following modes:

1. DCS Rising Edge

Stay as 1 after current selected clock rising edge, and the new select clock will be effective after its 1st rising edge, as shown in Figure 3-40.

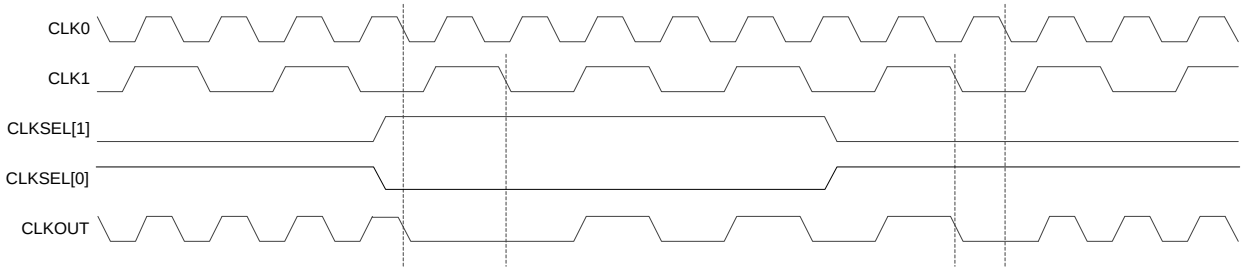
Figure 3-40 DCS Rising Edge



2. DCS Falling Edge

Stay as 0 after current selected clock falling edge, and the new select clock will be effective after its 1st falling edge, as shown in Figure 3-41.

Figure 3-41 DCS Falling Edge



3. Clock Buffer

In this mode, DCS acts as a Clock buffer.

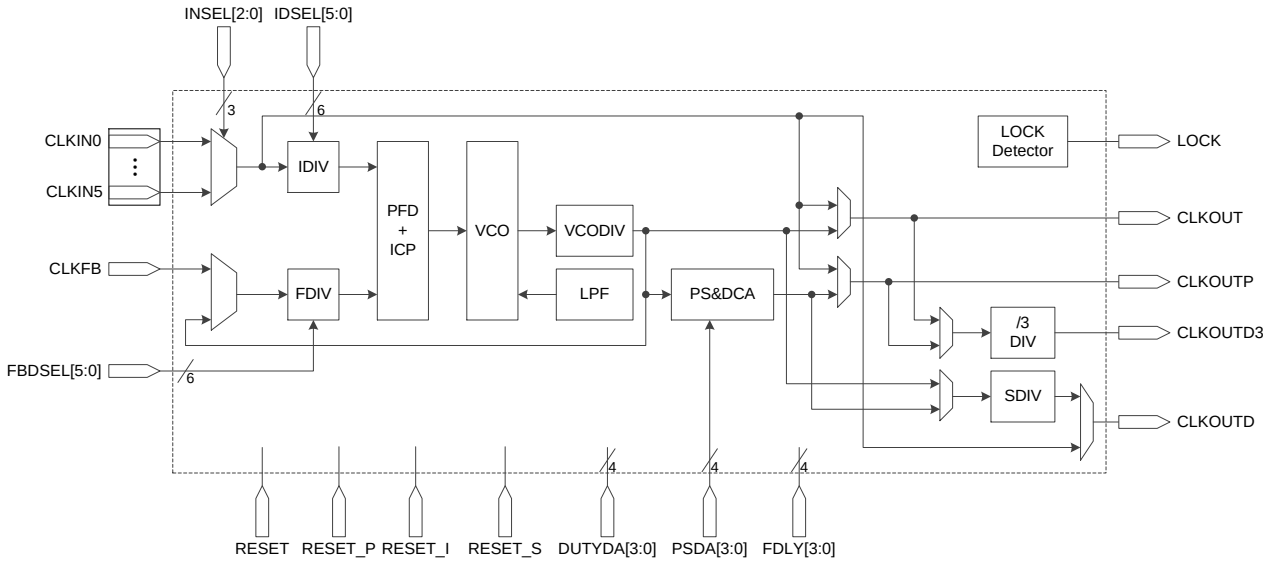
3.7.2 PLL

PLL (Phase-locked Loop) is one kind of a feedback control circuit. The frequency and phase of internal oscillator signal is controlled by the external input reference clock.

GW1N PLL blocks in GW1N series FPGA products provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted by parameters configuration.

Figure 3-42 shows PLL structure.

Figure 3-42 PLL Structure



PLL reference clock source can come from an external PLL pin or from internal routing GCLK, HCLK, or general data signal. PLL feedback signal can come from external PLL feedback input or from internal routing GCLK, HCLK, or general data signal.

PLL features are as follows:

- Input frequency:3MHz~450MHz
- VCO vibration frequency:400MHz~900MHz

- CLKOUT output frequency: 3.125MHz~450MHz

PLL can adjust the frequency of input clock CLKIN (multiply and division). The formulas are as following:

1. $f_{CLKOUT} = (f_{CLKIN} * FDIV)/IDIV$
2. $f_{VCO} = f_{CLKOUT} * ODIV$
3. $f_{CLKOUTD} = f_{CLKOUT}/SDIV$
4. $f_{PFD} = f_{CLKIN}/IDIV = f_{CLKOUT}/FDIV$

Note！

- f_{CLKIN}: the frequency of input clock CLKIN
- f_{CLKOUT}: the clock frequency of CLKOUT and CLKOUTP
- $f_{CLKOUTD}$: the clock frequency of CLKOUTD, and CLKOUTD is the clock CLKOUT after division
- f_{PFD}: PFD Phase Comparison Frequency

Adjust IDIV, FDIV, ODIV, SDIV to get the clock with expected frequency.

Table 3-18 describes the PLL ports definition.

Table 3-18 PLL Ports Definition

Ports Name	I/O	Description
CLKIN [5:0]	I	Reference clock input
CLKFB	I	Feedback clock input
RESET	I	PLL reset
RESET_P	I	PLL Power Down
RESET_I	I	IDIV reset
RESET_S	I	SDIV and DIV3 reset
INSEL[2:0]	I	dynamic clock control selector: 0~5
IDSEL [5:0]	I	dynamic IDIV control: 1~64
FBDSEL [5:0]	I	dynamic FDIV control:1~64
PSDA [3:0]	I	dynamic phase control (rising edge effective)
DUTYDA [3:0]	I	dynamic duty cycle control (falling edge effective)
FDLY [3:0]	I	CLKOUTP dynamic delay control
CLKOUT	O	clcok outpout with no phase and duty cycle adjustment
CLKOUTP	O	clcok outpout with phase and duty cycle adjustment
CLKOUTD	O	clock divider from CLKOUT and CLKOUTP (controlled by SDIV)
CLKOUTD3	O	clock divider from CLKOUT and CLKOUTP (controlled by DIV3 with the constant division value 3)
LOCK	O	PLL lock status: 1 locked, 0 unlocked

3.7.3 HCLK

HCLK is the high-speed clock in GW1N series FPGA products, which can support high-speed data transfer. Its main purpose is for source synchronous data transfer protocols. See Figure 3-43 and Figure 3-44.

Figure 3-43 GW1N-1 HCLK Distribution

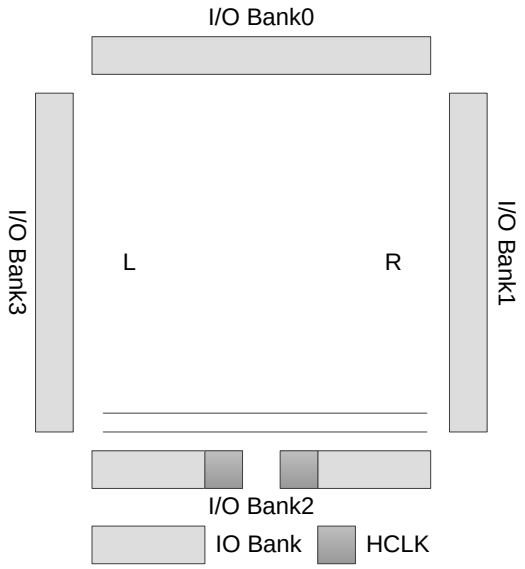
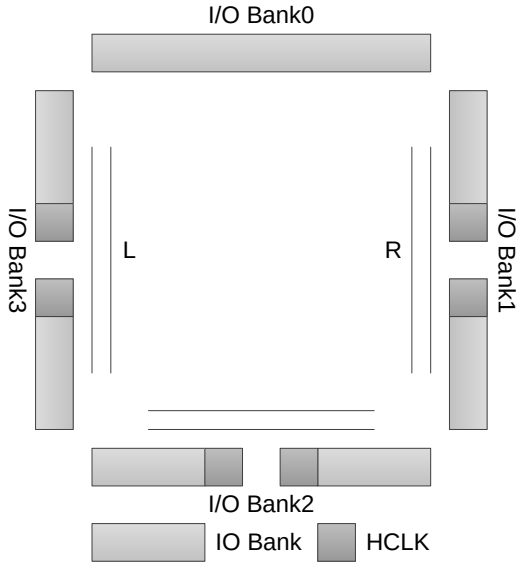


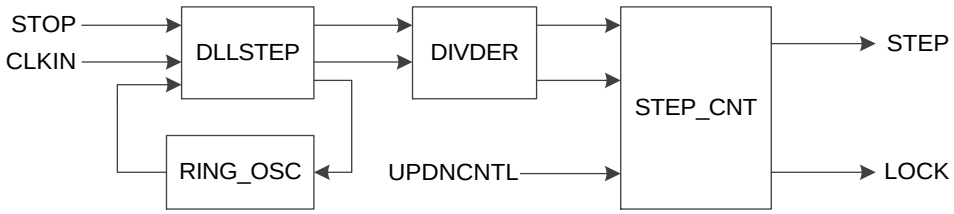
Figure 3-44 GW1N-2/4 HCLK Distribution



3.7.4 DLL

GW1N series FPGA products support DLL. For DLL function, see Figure 3-45.

Figure 3-45 GW1N DLL Function



The source of CLKIN can come from GCLKs and neighboring HCLKs.

STEP signal can be sent to the neighboring BANKs. For example, the STEP of DLL can be sent to HCLK in BANK2. At the same time, the signal STEP can also be sent to user logic through CRU.

3.8 Long Wire (LW)

As a supplementary to CRU, GW1N series FPGA products provides another routing resource- Long Wire, which can be used as clock, clock enable, set/reset,or other high fan out signals.

3.9 Global Set/Reset (GSR)

A global Set/Rest (GSR) network is built in GW1N series FPGA product. There is a direct connection to core logic. It can be used as asynchronous/synchronous set or asynchronous/synchronous reset. The registers in CFU and I/O can be individually configured to use GSR.

3.10 Configuration

GW1N series FPGA products support SRAM and Flash. GW1N configuration supports on chip Flash and off chip Flash. GW1N series

FPGA products support DUAL BOOT, providing a selection for users to backup data to off chip Flash according to requirements.

GW1N series FPGA products support not only JTAG, but also Gowin Semiconductor own configuration mode GowinCONFIG: AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, and CPU. All the devices support JTAG and AUTO BOOT. For the detailed information, please refer to *GW1N series FPGA Products Programming and Configureation User Guide*.

3.10.1 SRAM Configuration

When you adopt SRAM to configure, each time device is powered on, it needs to download the bit stream file to configure.

3.10.2 Flash Configuration

Flash configuration data is stored in on-chip Flash. Each time device is powered on, the configuration data transfers from the flash to SRAM, which controls the working of the device. This can complete configuration within a few ms.This mode is called “Quick Start”. GW1N series FPGA products also support off chip Flash configuration and dual-boot. Please refer to *GW1N series FPGA Products Programming and Configureation User Guide* for the detailed information.

3.11 On Chip Oscillator

There is an internal Oscillator in each GW1N series FPGA product. During the configuration, it can provide clock for MSPI mode. Table 3-19 describes the output frequency.

Table 3-19 Oscillator Output Frequency Options

Mode	Frequency	Mode	Frequency	Mode	Frequency
0	2.5MHz[1]	8	7.8MHz	16	15.6MHz
1	5.4MHz	9	8.3MHz	17	17.9MHz
2	5.7MHz	10	8.9MHz	18	21MHz
3	6.0MHz	11	9.6MHz	19	25MHz
4	6.3MHz	12	10.4MHz	20	31.3MHz
5	6.6MHz	13	11.4MHz	21	41.7MHz
6	6.9MHz	14	12.5MHz	22	62.5MHz
7	7.4MHz	15	13.9MHz	23	125MHz[2]

Note！

- [1] Default Frequency is 2.5 MHz.
- [2] 125MHz is too fast for MSPI.

On Chip Oscillator also provides clock resource for user designs. Up to 64 clock frequencies can be obtained by setting parameters. The following formuals are used to get the output clock frequency:

f_{out}=250MHz/Param

“Param” is the configuration parameter with the range 2~128, and supports even number only.

4 AC/DC Characteristic

4.1 Operating conditions

Table 4-1 Absolute Max. Ratings

Name	Description	Min.	Max.
V_{CC}	LV: Core Power	-0.5V	1.32V
	UV:Core Power	-0.5V	3.75V
V_{CCO}	I/O Bank Power	-0.5V	3.75V
V_{CCX}	Auxiliary Power	-0.5V	3.75V
Operating Temperature (Industrial)	Operating Temperature	-40℃	+125℃
Storage Temperature	Storage Temperature	-65℃	+150℃

Table 4-2 Recommended Operating Conditions

Name	Description	Min.	Max.
V_{CC}	LV: Core Power	1.14V	1.26V
	UV:Core Power	1.71V	3.465V
V_{CCO}	I/O Bank Power	1.14V	3.6V
V_{CCX}	Auxiliary Power	2.3V	3.465V
T_{JCOM}	Junction temperature Commercial operation	0℃	+85℃
T_{JIND}	Junction temperature Industrial operation	-40℃	+100℃
T_{RAMP}	Power supply ramp rates for all power supplies	0.01mV/μs	10mV/μs

Table 4-3 Hot Socket Specifications

Name	Description	Condition	Max.
I_{HS}	(Input or I/O leakage current)	$0<V_{IN}<V_{IH}$ (MAX)	TBD

4.2 ESD

Table 4-4 GW1N ESD - HBM

Device	GW1N-1	GW1N-2	GW1N-4	GW1N-6	GW1N-9
LQ100	HBM>1,000V	HBM>1,000V	HBM>1,000V	-	-
LQ144	HBM>1,000V	HBM>1,000V	HBM>1,000V	HBM>1,000V	HBM>1,000V
MG160	HBM>1,000V	HBM>1,000V	HBM>1,000V	HBM>1,000V	HBM>1,000V
PG204	HBM>1,000V	-	-	-	-
PG256	-	HBM>1,000V	HBM>1,000V	HBM>1,000V	HBM>1,000V
UG332	-	-	-	HBM>1,000V	HBM>1,000V
QN32	HBM>1,000V	-	-	-	-
CS30	TBD	-	-	-	-
CS72	-	TBD	TBD	-	-

Table 4-5 GW1N ESD - CDM

Device	GW1N-1	GW1N-2	GW1N-4	GW1N-6	GW1N-9
LQ100	CDM>500V	CDM>500V	CDM>500V	-	-
LQ144	CDM>500V	CDM>500V	CDM>500V	CDM>500V	CDM>500V
MG160	CDM>500V	CDM>500V	CDM>500V	CDM>500V	CDM>500V
PG204	CDM>500V	-	-	-	-
PG256	-	CDM>500V	CDM>500V	CDM>500V	CDM>500V
UG332	-	-	-	CDM>500V	CDM>500V
QN32	CDM>500V	-	-	-	-
CS30	TBD	-	-	-	-
CS72	-	TBD	TBD	-	-

Table 4-6 DC Electrical Characteristics over Recommended Operating Conditions

Name	Description	Condition	Min.	Typ.	Max.
I_{IL},I_{IH}	Input or I/O leakage	$V_{CCO}<V_{IN}<V_{IH}$ (MAX)	-	-	210μA
		$0V<V_{IN}<V_{CCO}$	-	-	10μA
I_{PU}	I/OActive Pull-up Current	$0<V_{IN}<0.7V_{CCO}$	-30μA	-	-150μA
I_{PD}	I/OActive Pull-down Current	V_{IL} (MAX)$<V_{IN}<V_{CCO}$	30μA	-	150μA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN}=V_{IL}$ (MAX)	30μA	-	-
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN}=0.7V_{CCO}$	-30μA	-	-
I_{BHLO}	Bud HoldLow Overdrive Current	$0\leq V_{IN}\leq V_{CCO}$	-	-	150μA
I_{BHHO}	BusHoldHigh Overdrive Current	$0\leq V_{IN}\leq V_{CCO}$	-	-	-150μA
V_{BHT}	Bus hold trip points		V_{IL} (MAX)	-	V_{IH} (MIN)
C1	I/O Capacitance			5pF	8pF

Name	Description	Condition	Min.	Typ.	Max.
V_{HYST}	Hysteresis for Schmitt Trigge inputs	V_{CCO}=3.3V, Hysteresis= Large	-	482mV	-
		V_{CCO}=2.5V, Hysteresis= Large	-	302mV	-
		V_{CCO}=1.8V, Hysteresis= Large	-	152mV	-
		V_{CCO}=1.5V, Hysteresis= Large	-	94mV	-
		V_{CCO}=3.3V, Hysteresis= Small	-	240mV	-
		V_{CCO}=2.5V, Hysteresis= Small	-	150mV	-
		V_{CCO}=1.8V, Hysteresis= Small	-	75mV	-
		V_{CCO}=1.5V, Hysteresis= Small	-	47mV	-

Table 4-7 Static Supply Current

Name	Description	LV/UV	Device	Typical
I_{CC}	Core current V_{CCX}=3.3V, V_{CCX}=2.5V	LV	GW1N-1	1.8mA (test data)
I_{CCX}	V_{CCX} current（V_{CCX}=3.3V)	LV	GW1N-1	1mA (test data)
	V_{CCX} current (V_{CCX}=2.5V)	LV	GW1N-1	0.8mA (test data)
I_{CCO}	I/O Bank current (V_{CCO}=2.5V)	LV	ALL	-

4.3 DC Characteristic

Table 4-8 I/O Operating Conditions Recommended

Name	Output V_{CCO} (V)			Input V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL33	3.135	3.3	3.465	-	-	-
LVCMOS33	3.135	3.3	3.465	-	-	-
LVCMOS25	2.375	2.5	2.625	-	-	-
LVCMOS18	1.71	1.8	1.89	-	-	-
LVCMOS15	1.425	1.5	1.575	-	-	-
LVCMOS12	1.14	1.2	1.26	-	-	-
SSTL15	1.425	1.5	1.575	0.68	0.75	0.9
SSTL18_I	1.71	1.8	1.89	0.833	0.9	0.969
SSTL18_II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I	2.375	2.5	2.645	1.15	1.25	1.35
SSTL25_II	2.375	2.5	2.645	1.15	1.25	1.35
SSTL33_I	3.135	3.3	3.465	1.3	1.5	1.7
SSTL33_II	3.135	3.3	3.465	1.3	1.5	1
HSTL18_I	1.71	1.8	1.89	0.816	0.9	1.08
HSTL18_II	1.71	1.8	1.89	0.816	0.9	1.08
HSTL15	1.425	1.5	1.575	0.68	0.75	0.9
PCI33	3.135	3.3	3.465	-	-	-
LVPECL33E	3.135	3.3	3.465	-	-	-
MLVDS25E	2.375	2.5	2.625	-	-	-
BLVDS25E	2.375	2.5	2.625	-	-	-
RSDS25E	2.375	2.5	2.625	-	-	-
LVDS25E	2.375	2.5	2.625	-	-	-
SSTL15D	1.425	1.5	1.575	-	-	-
SSTL18D_I	1.71	1.8	1.89	-	-	-
SSTL18D_II	1.71	1.8	1.89	-	-	-
SSTL25D_I	2.375	2.5	2.625	-	-	-
SSTL25D_II	2.375	2.5	2.625	-	-	-
SSTL33D_I	3.135	3.3	3.465	-	-	-
SSTL33D_II	3.135	3.3	3.465	-	-	-
HSTL15D	1.425	1.575	1.89	-	-	-
HSTL18D_I	1.71	1.8	1.89	-	-	-
HSTL18D_II	1.71	1.8	1.89	-	-	-

Table 4-9 IOB Single - Ended DC Electrical Characteristic

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max				
LVCMOS33 LVTTL33	-0.3V	0.8V	2.0V	3.6V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
							24	-24
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS25	-0.3V	0.7V	1.7V	3.6V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS18	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.6V	0.4V	V_{CCO}.0.4V	4	-4
							8	-8
							12	-12
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS15	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.6V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS12	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.6V	0.4V	V_{CCO}-0.4V	2	-2
							6	-6
					0.2V	V_{CCO}-0.2V	0.1	-0.1
PCI33	-0.3V	0.3 x V_{CCO}	0.5 x V_{CCO}	3.6V	0.1 x V_{CCO}	0.9 x V_{CCO}	1.5	-0.5
SSTL33_I	-0.3V	V_{REF}-0.2V	V_{REF}+0.2V	3.6V	0.7	V_{CCO}-1.1V	8	-8
SSTL25_I	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	0.54V	V_{CCO}-0.62V	8	-8
SSTL25_II	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	NA	NA	NA	NA
SSTL18_II	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	3.6V	NA	NA	NA	NA
SSTL18_I	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
SSTL15	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
HSTL18_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
HSTL18_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA
HSTL15_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
HSTL15_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA

Table 4-10 I/O Differential Electrical Characteristics

LVDS25 (GW1N-1does not support.)

Name	Description	Condition	Min.	Typ.	Max.	Unit
V_{INA},V_{INB}	Input Voltage		0	-	2.4	V
V_{CM}	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	-	2.35	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	±100	-	-	mV
I_{IN}	Input Current	Power On or Power Off	-	-	±10	μA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100Ω	-	-	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100Ω	0.9	-	-	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low		-	-	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100Ω	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between High and Low		-	-	50	mV
I_S	Short-circuit current	V_{OD} = 0V output short-circuit	-	-	15	mA

4.4 Switching Characteristic

4.4.1 Internal Switching Characteristics

Table 4-11 CFU Block Internal Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{LUT4_CFU}	LUT4 delay	-	0.674	ns
t_{LUT5_CFU}	LUT5 delay	-	1.388	ns
t_{LUT6_CFU}	LUT6 delay	-	2.01	ns
t_{LUT7_CFU}	LUT7 delay	-	2.632	ns
t_{LUT8_CFU}	LUT8 delay	-	3.254	ns
t_{SR_CFU}	Set/Reset to Register output	-	1.86	ns
t_{CO_CFU}	Clock to Register output	-	0.76	ns

Table 4-12 B-SRAM Internal Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{COAD_BSRAM}	Clock to output from read address/data	-	5.10	ns
t_{COOR_BSRAM}	Clock to output from output register	-	0.56	ns

Table 4-13 DSP Internal Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{COIR_DSP}	Clock to output from input register	-	4.80	ns
t_{COPR_DSP}	Clock to output from pipeline register	-	2.40	ns
t_{COOR_DSP}	Clock to output from output register	-	0.84	ns

4.4.2 External Switching Characteristics

Table 4-14 External Switching Characteristics

Name	Description	Device	-5		-6		Unit
			Min.	Max.	Min.	Max.	
Clocks	TBD	TBD	TBD	TBD	TBD	TBD	
Pin-LUT-Pin Delay	TBD	TBD	TBD	TBD	TBD	TBD	
General I/O Pin Parameters	TBD	TBD	TBD	TBD	TBD	TBD	

Table 4-15 On chipOscillator Output Frequency

Name	Description	Min.	Typ.	Max.
f_{MAX}	Output Frequency (0 to +85℃)	106.25MHz	125MHz	143.75MHz
	Output Frequency (-40 to +100℃)	100MHz	125MHz	150MHz
t_{DT}	Clock Duty Cycle	43%	50%	57%
t_{OPJIT}	Clock Period Jitter	0.01UIPP	0.012UIPP	0.02UIPP

4.5 User Flash Characteristic

4.5.1 DC Characteristic [1]

(T_J = -40~+100℃, V_{CC} = 1.08~1.32V, V_{CCX} = 1.62~3.63V, V_{SS} = 0V)

Table 4-16 User Flash DC Characteristic

Name	Parameter	Max.		Unit	Wake-up Time	Condition
		V_{CC}[3]	V_{CCX}			
Read mode (w/I 25ns)[1]	I_{CC1}[2]	2.19	0.5	mA	NA	Min. Clcok period, duty cycle 100%, VIN = “1/0”
Write mode		0.1	12	mA	NA	
Erase mode		0.1	12	mA	NA	
Page erase mode		0.1	12	mA	NA	
Read mode static current (25-50ns)	I_{CC2}	980	25	μA	NA	XE=YE=SE=“1”, between T=T_{acc} and T=50ns, I/O=0mA; later than T=50ns, read mode is turned off, and I/O current is the current of standby mode.
Standby mode	I_{SB}	5.2	20	μA	0	V_{SS}, V_{CCX}, and V_{CC}

Note!

- [1] means the average current, and the peak value is higher than the average one.
- [2] Caculated in different T_{new} clock periods.
  - $T_{new} < T_{acc}$ is not allowed
  - $T_{new} = T_{acc}$
  - $T_{acc} < T_{new}$ - 50ns: I_{CC1} (new) = (I_{CC1} - I_{CC2})(T_{acc}/T_{new}) + I_{CC2}
  - T_{new}>50ns: I_{CC1} (new) = (I_{CC1} - I_{CC2})(T_{acc}/T_{new}) + 50ns x I_{CC2}/T_{new} + I_{SB}
  - t > 50ns, $I_{CC2} = I_{SB}$
- [3] V_{CC} must be greater than 1.08V from the zero wake-up time.

4.5.2 Timing Parameters[1,5,6]

(T_J = -40~+100℃, V_{CC} = 0.95~1.05V, V_{CCX} = 1.7~3.45V, V_{SS} = 0V)

Table 4-17 User Flash Timing Parameters

User Modes	Parameters	Name	Min.	Max.	Unit
Access time[2]	WC1	T_{acc}[3]	-	25	ns
	TC		-	22	ns
	BC		-	21	ns
	LT		-	21	ns
	WC		-	25	ns
Program/Erase to data storage		T_{nvs}	5	-	μs
Data storage hold time		T_{nvh}	5	-	μs
Data storage hold time (Overall erase)		T_{nvh1}	100	-	μs
Time from data storage to program setup		T_{pgs}	10	-	μs
Program hold time		T_{pgh}	20	-	ns
Program time		T_{prog}	8	16	μs
Erase ready time		T_{wpr}	>0	-	ns
Erase hold time		T_{whd}	>0	-	ns
Time from control signal to write/Erase setup		T_{cps}	-10	-	ns
Time from SE to read setup		T_{as}	0.1	-	ns
E pulse high level time		T_{pws}	5	-	ns
Adress/data setup time		T_{ads}	20	-	ns
Adress/data hold time		T_{adh}	20	-	ns
Data hold time		T_{dh}	0.5	-	ns
Read mode address hold time[3]	WC1	T_{ah}	-	25	ns
	TC		-	22	ns
	BC		-	21	ns
	LT		-	21	ns
	WC		-	25	ns
SE pulse low level time		T_{nws}	2	-	ns
Recovery time		T_{rcv}	10	-	μs
Data storage time		T_{hv}[4]	-	6	ms
Erase time		T_{erase}	100	120	ms
Overall erase time		T_{me}	100	120	ms
wake-up time from power down to standby mode		T_{wk_pd}	7	-	μs
Standby hold time		T_{sbh}	100	-	ns
V_{CC} setup time		T_{ps}	0	-	ns
V_{CCX} hold time		T_{ph}	0	-	ns

Note！

- [1] The parameter values may change.
- [2] The values are simulation data only.
- [3]After XADR, YADR, XE, and YE are valid, T_{acc} start time is SE rising edge. DOUT is kept until the next valid read operation.
- [4]T_{hv} is the time between write and the next erasure.The same address can not be written twice before erasure, so does the same register. This limitation is for safety.
- [5]Both the rising edge time and falling edge time for all waveform is 1ns.
- [6] TX, YADR, XE and YE hold time need to be T_{acc} at leaset, and T_{acc} start from SE rising edge.

4.5.3 Operation Timing Diagrams

Figure 4-1 GW1N User Flash Read Operation

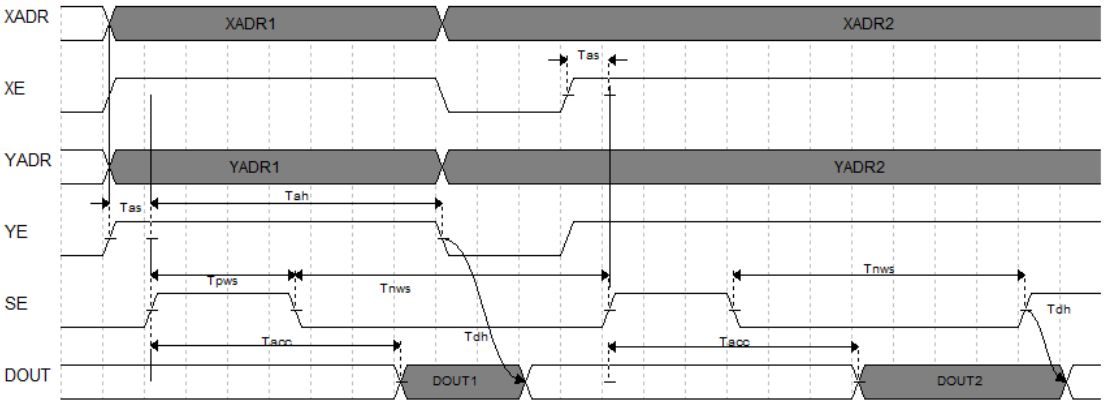


Figure 4-2 GW1N User Flash Program Operation

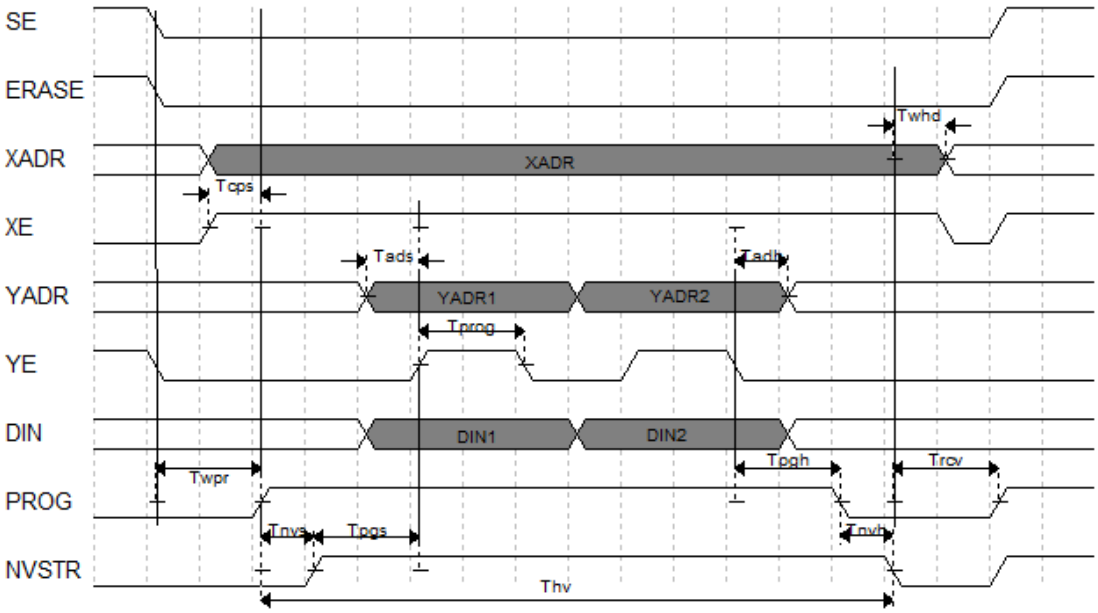
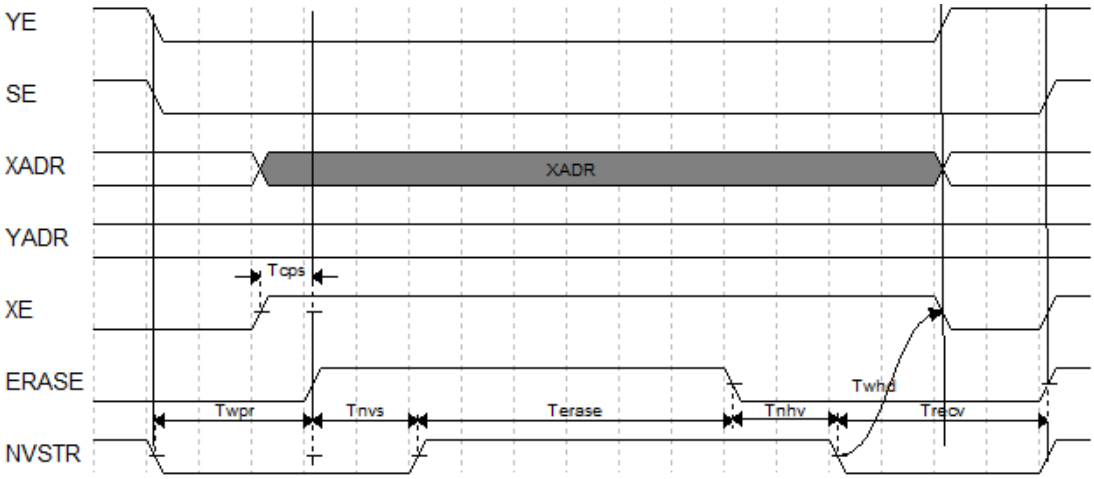


Figure 4-3 GW1N User Flash Erase Operation



4.6 Configuration Interface Timing Specification

GW1N series FPGA products GowinCONFIG support 6 configuration modes: AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, and CPU. For detailed information, please refer to *GW1N series FPGA Products Programming and Configureation User Guide*.

4.6.1 JTAG Port Timing Specifications

JTAG mode of GW1N series FPGA products complies with IEEE1532 and IEEE1149.1 boundary scan standard.

JTAG mode downloads the bitstream to SRAM, and the data is lost after power off.

Figure 4-4 shows JTAG timing.

Figure 4-4 JTAG Timing

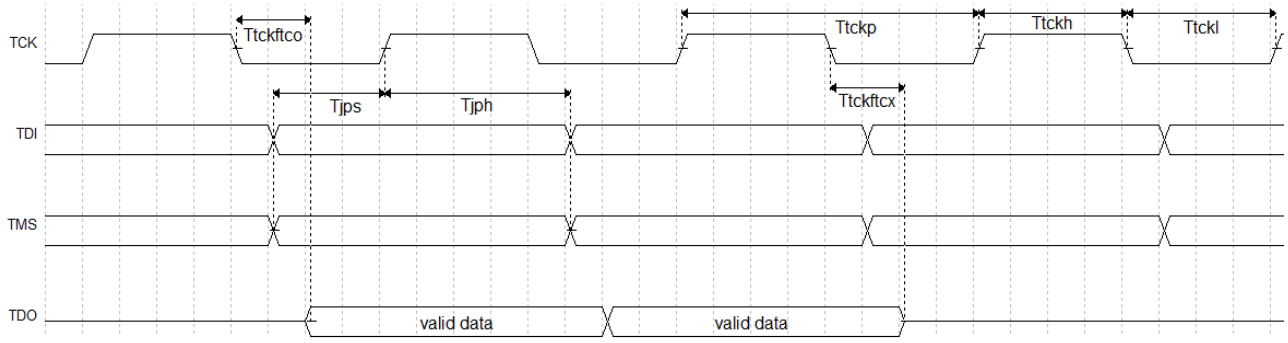


Table 4-18 JTAG Timing Parameters

Name	Description	Min.	Max.
$T_{tckftco}$	Time from TCK falling edge to output		10ns
$T_{tckftcx}$	Time from TCK falling edge to high impedance		10ns
T_{tckp}	TCK clock period	40ns	-
T_{tckh}	TCK clock high time	20ns	-
T_{tckl}	TCK clock low time	20ns	-
T_{jps}	JTAG PORT setup time	10ns	
T_{jph}	JTAG PORT hold time	8ns	

Other than the power requirements, the following conditions need to be met to use MSPI configuration mode:

- MSPI port enable
  Set RECONFIG_N as “NON-RECOVERY” for the first programming after power up or the previous programming.
- Initiate new program
  Power recycle or provide one low pulse for programming pin RECONFIG_N.

4.6.2 AUTO BOOT Port Timing Specifications

AUTOBOOT is one mode with instant-on feature for GW1N series FPGA products. In this mode, FPGA reads data from the on chip Flash directly for the program to load after the chip is powered on.

On chip Flash is configured via JTAG interface. After the configuration, RECONFIG_N is triggered by low level pulse, or auto boot configuration starts after power recycle. Figure 4-5 shows the timing.

Figure 4-5 Power Recycle Timing

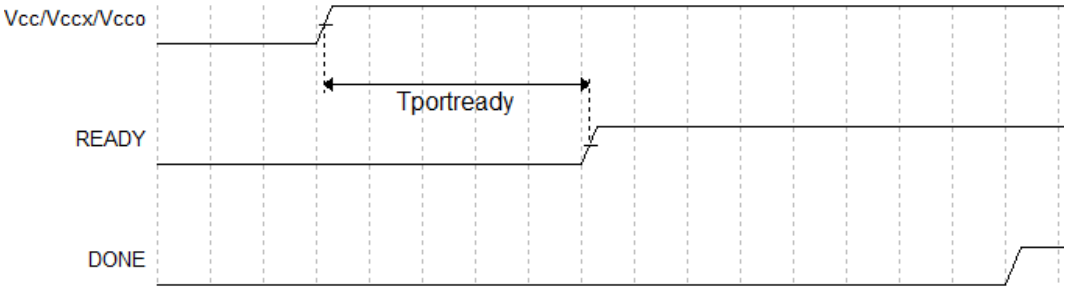


Figure 4-6 RECONFIG_N Trigger Timing

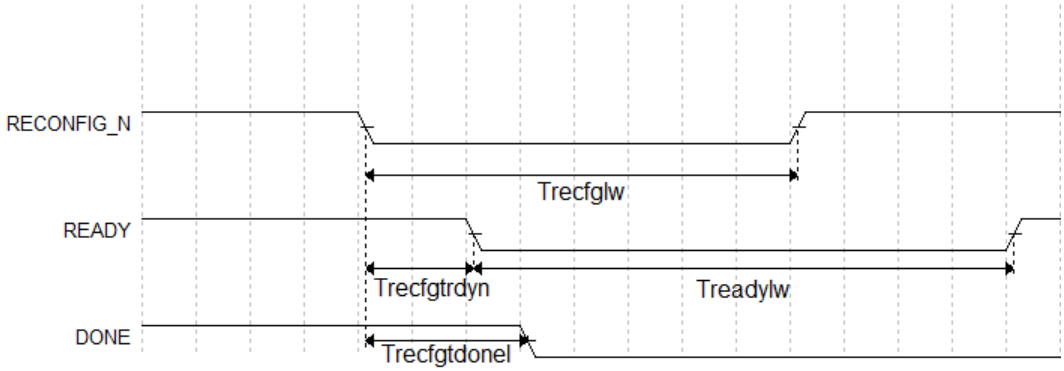


Table 4-19 shows the related timing parameters.

Table 4-19 Parameters for Power Recycle and RECONFIG_N Trigger Timing

Name	Description	Min.	Max.
$T_{portready}$	Time from application of V_{CC}, V_{CCX} and V_{CCO} to the rising edge of READY	-	23ms
$T_{recfglw}$	RECONFIG_N low pulse width	25ns	
$T_{recfgtrdyn}$	Time from RECONFIG_N falling edge to READY low	-	70ns
$T_{readylw}$	READY low pulse width	TBD	
$T_{recfgtdonel}$	Time from RECONFIG_N falling edge to DONE low	-	80ns

4.6.3 SSPI Port Timing Specifications

In the slave SSPI mode, GW1N series FPGA products are configured by hardware processer via SPI.

Figure 4-7 shows SSPI timing diagram.

Figure 4-7 SSPI Timing Diagram

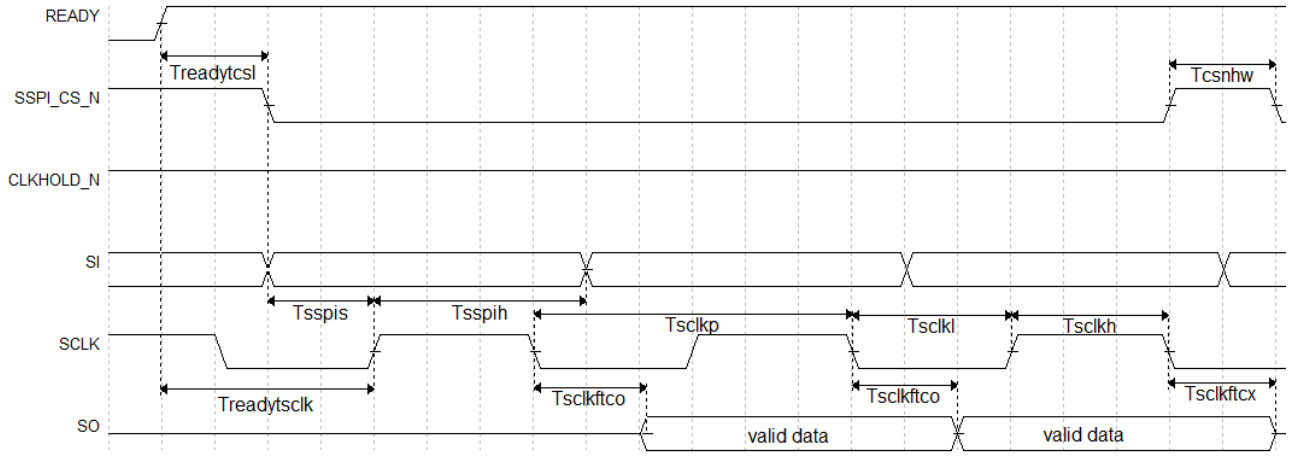


Table 4-20 describes the timing parameters.

Table 4-20 SSPI Timing Parameters

Name	Description	Min.	Max.
T_{sclkp}	SCLK clock period	15ns	-
T_{sclkh}	SCLK clock high time	7.5ns	-
T_{sclkl}	SCLK clock low time	7.5ns	-
T_{sspis}	SSPI PORT setup time	2ns	-
T_{sspih}	SSPI PORT hold time	0ns	-
$T_{sclkftco}$	Time from SCLK falling edge to output	-	10ns
$T_{sclkftcx}$	Time from SCLK falling edge to high impedance	-	10ns
T_{csnhw}	CSN high time	25ns	-
$T_{readytcsl}$	Time from READY rising edge to CSN low		
$T_{readytsclk}$	Time from READY rising edge to first SCLK edge	TBD	-

Other than the power requirements, the following conditions need to be met to use SSPI configuration mode:

- SSPI port enable
  Set RECONFIG_N as “NON-RECOVERY” for the first programming after power up or the previous programming.
- Initiate new program
  Power recycle or provide one low pulse for programming pin RECONFIG_N.

4.6.4 MSPI Port Timing Specifications

In master MSPI mode, the configuration data is retrieved automatically from the off chip SPI Flash.

After MSPI writes the configuration data to the off chip Flash, power recycle or RECONFIG_N will trigger device configuration.

Figure 4-8 MSPI Timing Diagram

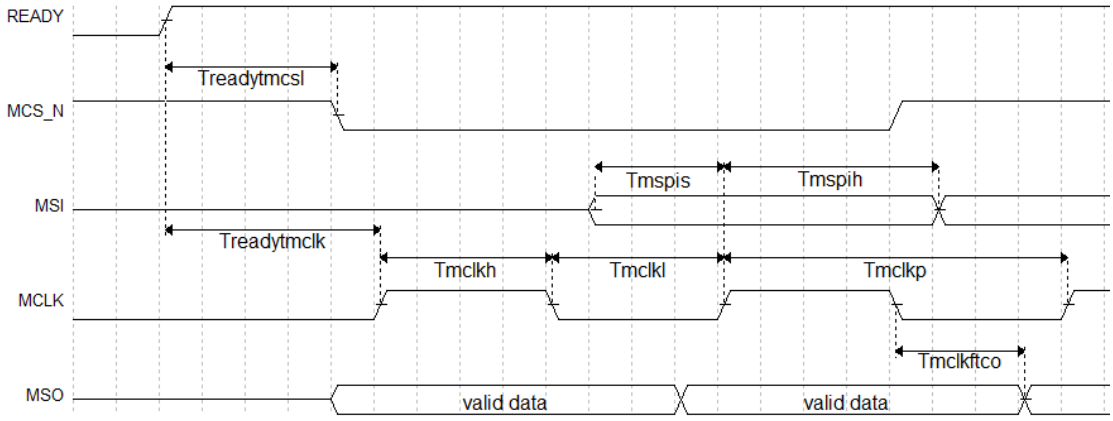


Table 4-21 describes the timing parameters.

Table 4-21 MSPI Timing Parameters

Name	Description	Min.	Max.
T_{mclkp}	MCLK clock period	15ns	-
T_{mclkh}	MCLK clock high time	7.5ns	-
T_{mclkl}	MCLK clock low time	7.5ns	-
T_{mspis}	MSPI PORT setup time	5ns	-
T_{mspih}	MSPI PORT hold time	1ns	-
$T_{mclkftco}$	Time from MCLK falling edge to output	-	10ns
$T_{readytmcsl}$	Time from READY rising edge to MCS_N low	100ns	200ns
$T_{readytmclk}$	Time from READY rising edge to first MCLK edge	2.8μs	4.4μs

4.6.5 DUAL BOOT

In DUAL BOOTmode, the configuration data is retrieved automatically from the off chip Flash or from on chip Flash.

GW1N series FPGA products try to configure first from the on chip Flash memory. If there is no data in the on chip Flash or the configuration fails, the device attempts to configure from the off chip Flash memory. If that too fails, the device cannot work.

4.6.6 CPU

In CPU mode, GW1N series FPGA products are configured by hardware processor via DBUS interface. Other than the power requirements, the following conditions need to be met to use CPU configuration mode:

- CPU port enable
  Set RECONFIG_N as “NON-RECOVERY” for the first programming after power up or the previous programming.
- Initiate new program
  Power recycle or provide one low pulse for programming pin RECONFIG_N.

4.6.7 SERIAL

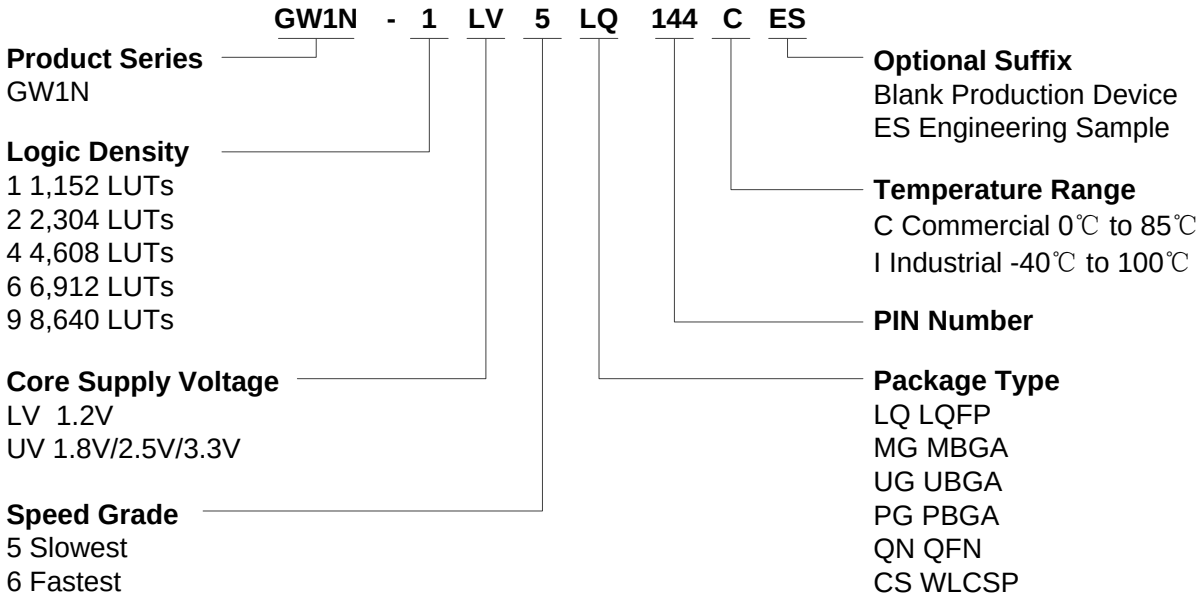
In SERIAL mode, GW1N series FPGA products are configured by hardware processor via serial interface. Other than the power requirements, the following conditions need to be met to use SERIAL configuration mode:

- SERIAL port enable
  Set RECONFIG_N as “NON-RECOVERY” for the first programming after power up or the previous programming.
- Initiate new program
  Power recycle or provide one low pulse for programming pin RECONFIG_N.

5 Ordering Information

5.1 Part Name

Figure 5-1 Part Name



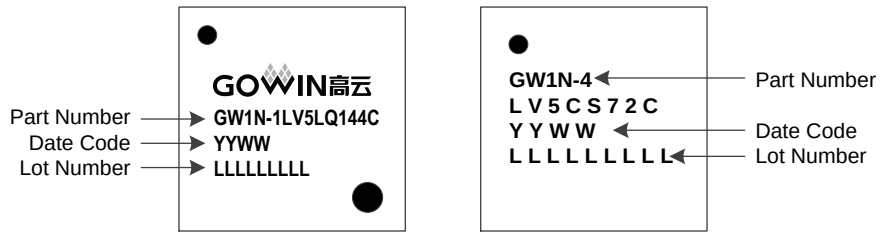
Note!

- QN and CS package support LV only.
- Speed Grade is used for both LV and UV.

5.2 Package Mark

The device information of Gowin Semiconductor is marked on the chip surface, as shown in Figure 5-2.

Figure 5-2 Package Mark



Note!

The first two lines of the right figure above are “Part Number”.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